UK Semiconductor Infrastructure Initiative Feasibility Study

Summary of findings

31 October 2023

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Department of Engineering

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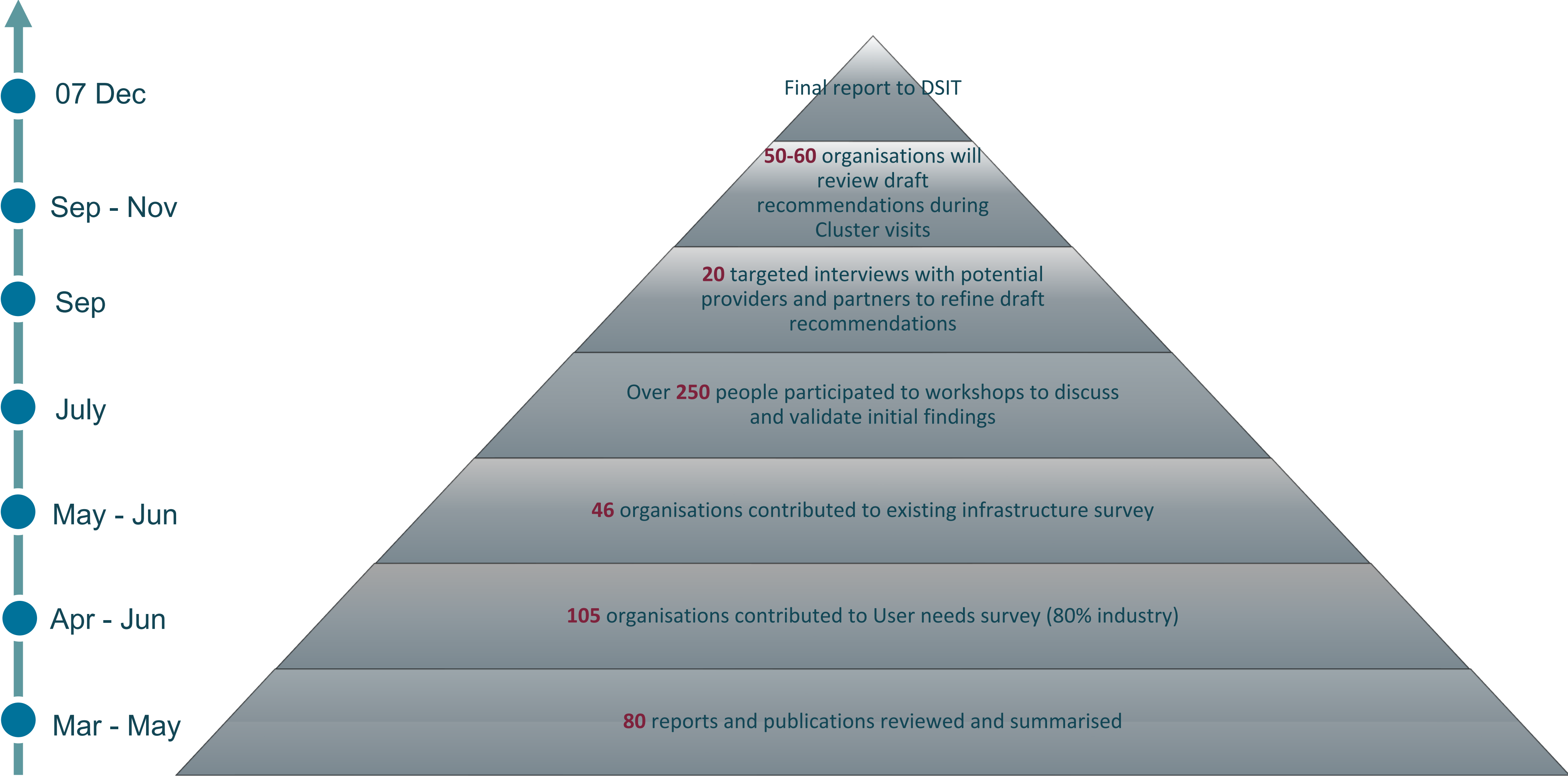
UK Semiconductor Infrastructure Initiative

- The newly formed Department for Science, Innovation and Technology (DSIT) has commissioned a study to understand the **technical** and **economic** feasibility of developing specific capabilities to support **commercial R&D**, grow the UK semiconductor sector and contribute to supply chain resilience.
  - WP1 - Silicon manufacturing capability to support prototyping
  - WP2 - Advanced packaging capability
  - WP3 - Compound open-access foundry capability
  - WP4 - Design IP/tooling capability
  - WP5 - Strategic coordination capability that would provide an institutional framework around the infrastructure components

Process for evidence gathering and timeline



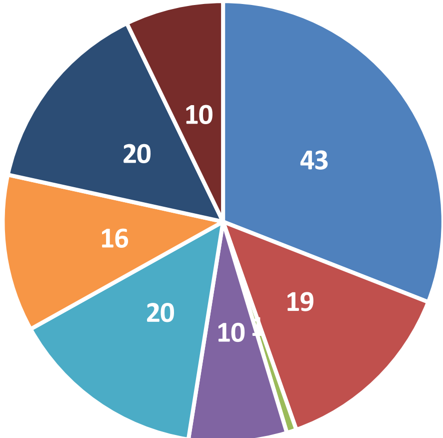
WP1 - Silicon manufacturing capability to support prototyping

Silicon manufacturing capability to support prototyping – User Needs

Important process technologies

(values represent number of organisations)

- Bulk CMOS
- FDSOI
- PDSOI
- Bi-CMOS
- High Voltage/Power
- FinFET
- Si-based photonics
- Si-based Image sensors



59 organisations responded

Types of chips and the node sizes required

(Ignoring the totals, the figure in each cell represents number of organisations requiring a type of IC at a particular node size. The totals indicate overall level of need)

		Node sizes								
		>90nm	90-65nm	45-28nm	22-20nm	18-10nm	7-5nm	3nm	<3nm	Total
Type of IC	Analog/mixed signal	18	14	16	14	5	6	3	1	77
	Digital	7	8	12	14	8	9	7	4	69
	Photonics	7	5	3	4	1	0	0	0	20
	MEMS	6	2	2	2	1	0	0	0	13
	Memory (including next generation)	4	3	4	6	6	5	3	1	32
	Total	42	32	37	40	21	20	13	6	

45 organisations responded

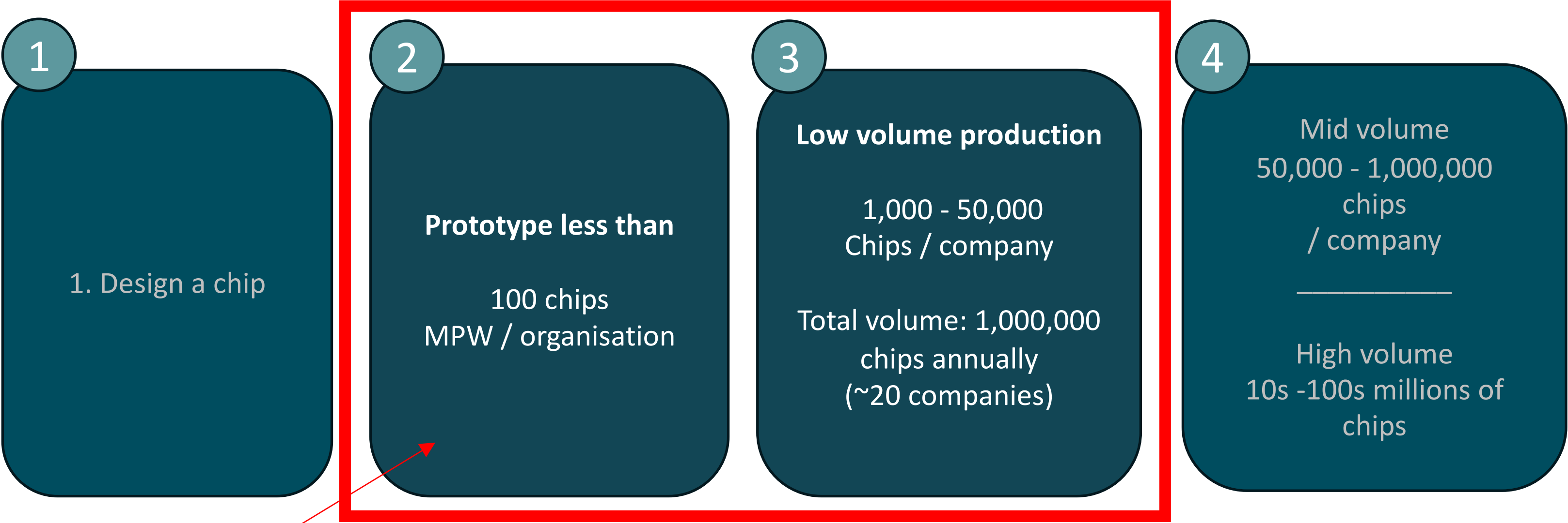
WP1 implementation model options

Implementation model category	Model 1 (CMOS in UK-based facility + post-processing in UK)		Model 3 (CMOS via overseas access + post-processing in UK)	'Do nothing' model
Implementation model option	1.1 - CMOS from UK facility **set up by the UK** (and built entirely by a UK entity); + Post-processing **in the same** UK facility	1.2 – CMOS from UK facility **set up by established foundry (e.g., GF);** + Post-processing **in the same** UK facility	3.1 - CMOS from overseas foundry, e.g., TSMC (via aggregator, IMEC); + Post-processing in a UK facility	Allow people to continue with what they presently do via established foundries (e.g., TSMC), aggregators (e.g., IMEC), and programmes (e.g., Europractice)
Node sizes	65-28nm	All node sizes? Depends on deal with established foundry (Down to 14nm, if GF?)		
Additional description	'Minimum viable fab' model - adequate for prototyping and low-volume manufacturing to meet UK demand	Scope and volume would be dependent on deal struck with established foundry	'Minimum viable fab' model - adequate for prototyping and low-volume manufacturing to meet UK demand	
Capability	Prototyping + Low-volume manufacturing	Prototyping + Low-volume manufacturing	Prototyping + Low-volume manufacturing	
Additional capabilities	+ Defence and other CNI sovereign capability; + supply chain resilience delivery as needed (limited)	+ Defence and other CNI sovereign capability; + supply chain resilience delivery as needed (limited)	+ Defence and other CNI sovereign capability; + supply chain resilience delivery as needed (limited)	
	+ Silicon photonics line (65nm) for prototyping and piloting in UK post-processing facility	+ Silicon photonics line (65nm) for prototyping and piloting in UK post-processing facility	+ Silicon photonics line (65nm) for prototyping and piloting in UK post-processing facility	
Additional comments	It would be beneficial to license the manufacturing process from an organisation that has good experience in setting up fabs and processes, e.g.. IMEC.	Might take a shorter time to establish that trying to do it ourselves (i.e., 1.1). Key question: would this be attractive to GF? This might require a sweetheart deal between the foundry and UK government (cf. Germany TSMC arrangement)	It is feasible for UK to buy CMOS chips and slots from TSMC. TSMC unlikely to be happy to deal with us directly due to low volumes, and ask us to deal with an aggregator, i.e., IMEC. (IMEC itself uses this approach. It gets its CMOS chips from TSMC and does the post-processing in-house)	

Assumptions

- In 1.1., the same equipment will be used for CMOS fabrication and post-processing.
  - Some additional equipment might be necessary for post-processing, e.g. sputtering for metalisation layers etc.
  - Therefore for 1.1., CMOS and post-processing would share majority of the equipment
- In 1.2., the post-processing would be in the same facility as the CMOS. However, the post-processing would be on a separate 'line'.
  - Therefore for 1.2, CMOS and post-processing will not be sharing equipment
- In all three models, Si Photonics would be in the same facility as CMOS post-processing.
  - There will be restrictions on which equipment can be shared between CMOS post-processing and Si Photonics to prevent cross-contamination.
  - Based on discussions, Si Photonics only requires 65nm. If equipment is to be shared, this assumes that Si Photonics will be done on non-critical lithography equipment (assuming critical lithography equipment goes down to 28nm)

Proposed scope of Silicon Prototyping and Piloting capability



Current estimates: 160 companies/ organisations in the UK

Purpose:

- Facilitate early-stage business prototyping
- Innovation on processes/additional functionality on CMOS

Purpose:

- Support early-stage scaling up of businesses
- Enable larger companies that want to design ASICs
- Allow production for niche markets and CNI/sovereign capability

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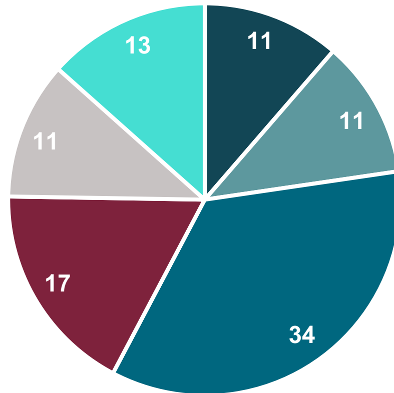
WP2 - Advanced packaging capability

Advanced packaging capability – User Needs

74 companies responded to Advanced Packaging part of the survey



NOW	Power	RF/Microwave	Photonics	Digital electronics	Sensors	Sum
Ceramic	5	6	7	2	4	**24**
Component	13	10	19	10	11	**63**
Metal	3	4	6	3	7	**23**
Plastics+	4	6	2	2	6	**20**
Grand Total	**25**	**26**	**34**	**17**	**28**	

FUTURE	Power	RF/Microwave	Photonics	Digital electronics	Sensors	Sum
Ceramic	2	3	3	0	1	**9**
Component	3	3	5	0	0	**11**
Hetro	1	1	1	0	0	**3**
Metal	1	0	2	0	0	**3**
Plastic+	1	2	2	2	2	**9**
Grand Total	**8**	**9**	**13**	**2**	**3**	

The values represent the total number of entries of materials processed in each packaging application area.

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Packaging testing requirements

Environmental e.g. humidity, temperature, thermal, moisture incl. accelerated environmental e.g. damp heat, life test, burn-in, accelerated stress test	Electrical, ESD	Mechanical testing (vibration, bump, shock)	Hermeticity, pressure, leak testing	Other (e.g. radiation cryogenic, RF characterisation, residual gas analysis, attachment strength)	Generic reliability (a combination of all others)
26	19	17	6	9	8

The values represent the total number of entries.* Total number of companies responded: **24

Top 3 challenges

Manufacturing challenges	• Shelf-life, cleanliness, precise application, temperature and humidity control, mechanical/optical stability of assembly equipment, deformation and heating, form factor, integration in wider system, etc. • Lack of equipment to exploit in volume
Innovativeness and R&D	• Development of novel materials for thermal management, conductivity and ease of use • Access to substrate design capability
Supply chain related challenges	• Long lead time for substrate delivery • Availability of silicon carbide as bare die for packaging without large minimum order quantities • General quality, reliability, and security of supply • Lead times of supply

Key market gaps and failures in respect to advanced packaging

1. Scale-up and translation from low to high volume

- Most UK companies focus on the high value design, prototyping and low volume production.
- Transition to volume challenges are finding automation partners, investment, low ROI.
- Only few players are doing high volume integration in UK, e.g., Seagate and CIL.

Current market adaptation:

1. Start-ups targeting volumes go to Asia (prompted by investors).
2. Asian integrators confirm potential interest when at volume but are not focused on design/ prototyping.
3. After Asian exploration, start-ups find way back to the UK packaging design houses.

Conclusion: Market failure is in efficiency of those start-up finding packaging design houses in the UK and affording their services.

Potential intervention on international collaboration:

- Streamline and actively facilitate steps 1-3, making it efficient to find partners in the UK and access the right volume packaging partners internationally.
- Make sure the volume packaging house know where to point folks to in the UK.
- It will help to retain the high value design capability in the UK.

Key market gaps and failures in respect to advanced packaging

2. Advanced Heterogeneous Integration

- There are players, who can do the 5 micron alignment required for generation one integration but not the order of magnitude higher alignment capability needed for next generation.
- Market failure is in availability of next generation chip-to-chip level vertical hetero integration with sub-micron alignment and volume (2.5 or 3D).
- Clear differentiation needed from the Si:Si hetero integration that is the focus of the main Asian fabs seeking to increase yield in lowest node Si with chiplets from single vendor.

Risks:

- Without next generation CS 2.5D+hetero capability, UK will increasingly fall behind in its integration capability jeopardising their ability to capture value from CS fab investment in the future.
- UK would become beholden to the designers and owners of the integration process dictating choice of CS chips.
- And to capture most from CS investment, next generation hetero is crucial as chips are increasingly deployed in combinations.

Proposed Heterogeneous Packaging Facility

The proposed scope of the technical capability is focused on **2.5D and 3D heterogeneous integration of differing materials (e.g. CS+Si, CS + CS, multi-vendor/-node Si)**. The offering is market agnostic and covers all application areas (RF, Optoelectronics, Power, Sensors and Digital electronics). Some of the packaged chip should be 'made-in-UK'. The facility should be funded by the UK government or PPI.

Auxiliary wafer processing and Deposition
The main requirement here is wafer processing, and in particular surface planarisation, wafer thinning and wafer bonding. In addition, there is a need for real deposition of barrier layers (e.g. by PECVD) and for metallisation (e.g. electroplating) for vias and interconnects.

Package/ System design and architecture
The significance of package design and system architecture is the foundational step in optimizing the performance, reliability, protection, size, cost, and time to market of semiconductor devices and modules. The expertise required is multi-disciplinary. This is where the UK excels and has the potential to lead in this domain.

Modelling
UK can have strategic advantage in commercial package design capability from main vendors with multi-physics model capabilities to tackle electro-thermal and mechanical properties and reliability modelling of packaging.

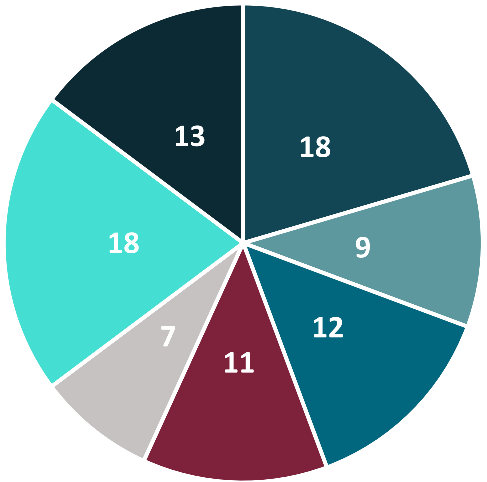
Assembly
Having an open access hetero package process modelling and assembly capability is crucial to transforming concepts into future proof prototypes and manufacturing. By co-locating resources, UK can expedite device and system development, rapidly bringing these processes to the industry. By investing in this capability, the UK can position itself as a global hub for package design and assembly process development.

Metrology
The metrology capability of the facility needs to encompass packaging integrity, integrity of electrical interconnects (voltage and current), adhesion of insulating material, alignment of fine pitch, surface metrology, inline metrology, automated alignment.

Testing, Reliability & Failure Analysis
An integrated test and assembly facility has both on-wafer and post-packing testing (accelerated, reliability, harsh environmental testing, including thermal, mechanical, electromagnetic and radiation). Optoelect-rical wafer level probe testing and leak testing of packaged devices are also important. There also need to be a suite of character-risation tools like XRD, EDX and SEM.

WP3 - Compound open-access foundry capability

Business types and size of the UK operations of the organisations responding to the Infrastructure user survey (for WP3)



**Values represent number of organisations (based on 69 responses).*

Revenue			
< £1.8 million	< £9 million	<£45 million	>£45 million
23	7	11	19

Location	Responses
East (England)	27
East Midlands (England)	3
London	7
North East (England)	8
North West (England)	5
Northern Ireland	4
Scotland	13
South East (England)	13
South West (England)	15
Wales	9
West Midlands	3
Yorkshire and The Humber	2

Compound open-access foundry capability – User Needs

Category	Current Materials	Future Materials
1	GaAs, GaSb, InGaAsP, InGaSb, InGaP, InP, InSb, Other III:Antimonides	GaAs, GaSb, GaP, InGaAs, InP, InSb, Bismides, GaAs with quantum dot, InP with quantum dot, Other III:Antomonides, Superlattices T2SL
2	GaN, Cubic Gallium Nitride, SiN, AlGaN	GaN, GaN on Diamond, SiN, Composites of nitrides with other functional materials
Others (3, 9, 11)	Chalcogenide materials (3) Thin film Lithium Niobate (9) Diamond (11) Metamaterials Copper Indium Gallium Sulphide	Chalcogenide materials (3) Thin film Lithium Niobate (9) Diamond (11) Metamaterials
4	Doped Graphene	
5 & 8	Silicon Photonics, SiGe	Ge, Ge on insulator
6	CMT	
7	SiC, Cubic SiC	SiC, Si on insulator
10	Ga2O3, AgO, BTO	Ga2O3, Thin film BTO

Current Compound Semiconductor Materials and their Applications

Category	Power	Photonics	RF/ Microwave	Digital electronics	Sensors	Total
1	1	23	8	2	7	41
2	9	7	10	1	3	30
3	1	3	0	2	1	7
4	1	1	1	0	1	4
5	0	1	3	0	0	4
6	0	1	0	0	1	2
7	10	1	0	1	1	13
10	2	2	0	0	0	4
Total	25	39	22	6	14	110

Future Compound Semiconductor Materials and their Applications

Category	Power	Photonics	RF/ Microwave	Digital electronics	Sensors	Total
1	1	3	10	1	5	20
2	9	11	4	0	2	26
3	1	1	3	1	1	7
5	0	0	1	0	1	2
7	9	1	2	2	2	16
10	3	0	2	0	0	5
Total	23	16	22	4	11	76

Opportunity map for identified "commercial" material sets

		Forecast	Applications	Opportunity?
SEGMENT 1 Arsenides etc	GaAs	\$4.1b (2028)	Quantum, telecoms, health, defence	Emerging markets coupled with new material processes (PDKs) and new devices
	GaSb	\$14m (2028, substrate)	GaSb can be used in infrared detectors, infrared LEDs and lasers and transistors, and thermal photovoltaic systems.	TBC
	InP	\$6.4b (2028) [1]	Quantum, telecoms, health, defence	Emerging markets coupled with new material processes (PDKs) and new devices
SEGMENT 2 Nitrides	GaN	RF GaN \$2.7B (2028) Power GaN \$2.04b (2028)	Telecoms, defence, Evs	TBC
	AlGaN	TBC	AlGaN finds applications in lasers, LEDs, UV detectors, and HEMTs.	TBC
SEGMENT 3 SiC	SiC	\$9b (2028)	EVs, LV grid	Difficult to define, as large scale SiC fabs are being built overseas
SEGMENT 4 Oxides	IGZO	TBC	Photonics, sensors, health, food, AI	Emerging markets coupled with new material processes (PDKs) and new devices Low volume fab facility already in UK
	Ga_2O_3	\$6m (2028, substrate)	EVs, LV grid	New material, requires research to create PDKs and commercial chips

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Note:
SEGMENTS 1 and 2 have lots of applications
SEGMENTS 3 and 4 have more specific applications

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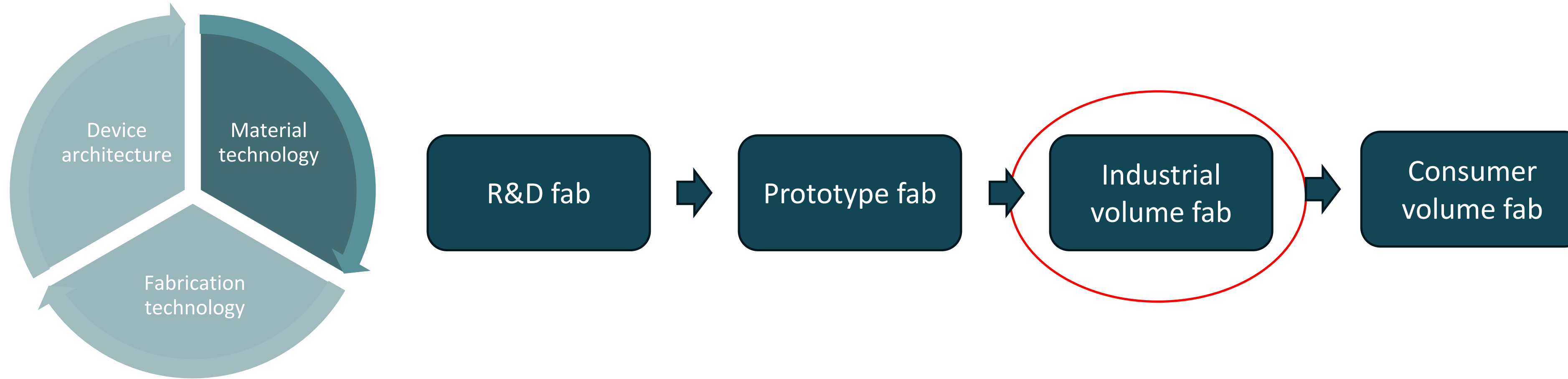
The fabrication flow for CS from innovation in small facilities to high volume production.



- The UK has recognised strengths in CS R&D but there is a gap in the subsequent route to commercialisation There is a need for a "bridge" to support the journey between developing CS devices to volume manufacture
- A single foundry cannot accommodate all compound semiconductor work
- Capability exists in the UK (not all open access) but the ecosystem is fragmented and investment is required

- Benefits of "*bridging the gap*"
  - Accelerate innovation towards volume production – faster turnaround, ease of design iteration
  - Create a clear route to commercialisation for UK R&D – no duplication of effort for volume
  - Attract inward investment to UK – pilot line with partner in UK, volume fab capability overseas
    - Proximity to design & materials R&D
  - Protect UK sovereign interests

CS “R&D with service offering” capability matrix

	Design	Prototyping	Pilot, Industrial volume fab production	Process yield improvement
SEGMENT 1 Arsenides, etc	Cardiff, Glasgow Uni, Semiwise, Sheffield, CISM?	Cardiff, JWNC/ KNT, CISM?		SmartNano NI
SEGMENT 2 Nitrides	Cardiff, Glasgow Uni, Semiwise, Cambridge, Sheffield, CISM?	Cardiff, JWNC/ KNT, Cambridge, CISM?		
SEGMENT 3 SiC	CISM, Warwick, Glasgow Uni, Semiwise	CISM		
SEGMENT 4 Oxides	Bristol, Southampton Uni			

Where do these fit?

- Others
- Queens

Observations

- UK activity in design and prototyping
- Lack of activity at scale-up

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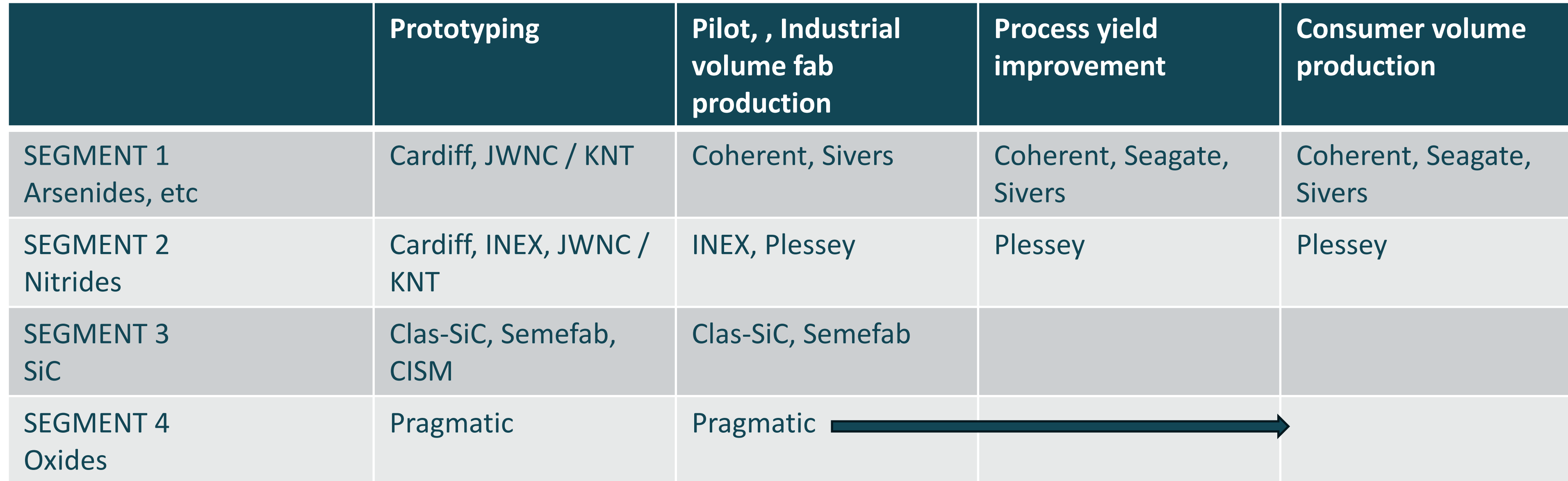
CS “commercial” capability matrix



	Prototyping	Pilot, , Industrial volume fab production	Process yield improvement	Consumer volume production
SEGMENT 1 Arsenides, etc	Cardiff, JWNC / KNT	Coherent, Sivers	Coherent, Seagate, Sivers	Coherent, Seagate, Sivers
SEGMENT 2 Nitrides	Cardiff, INEX, JWNC / KNT	INEX, Plessey	Plessey	Plessey
SEGMENT 3 SiC	Clas-SiC, Semefab, CISM	Clas-SiC, Semefab		
SEGMENT 4 Oxides	Pragmatic	Pragmatic →		

Where do these fit?

- Royce
- Sheffield

Observations
- UK activity in prototyping and pilot line production
- Less activity at volume production

CS foundry options

Intervention options	R&D fab	Prototype fab	Industrial volume fab/pilot	Consumer volume production	Revenue model	Comments
1. Incentivise capital investments to support prototyping - £100m	Universities	Existing capability e.g Glasgow, Springtown, Cardiff, Swansea, Newton Aycliffe etc.	Overseas	Overseas	License design / IP	Captures more value in UK, "industry standards", Provides 'back-up' small volume fabrication for defence
2. Repurpose existing facilities to create open-access CS foundry or foundries, dependent on material - £250m UK alone or with international partner?	Universities	Enhanced existing capability, coordinated with national semi institute	Enhanced existing capability, coordinated with national semi institute	1 Overseas 2 UK CS foundry 3 Inward investment	IP and manufacturing	Captures more value in UK Provides sovereign capability

Observations:

- Increased funding captures more value in the UK
- CS foundry may be capable of volume production, maybe in multiple locations by material

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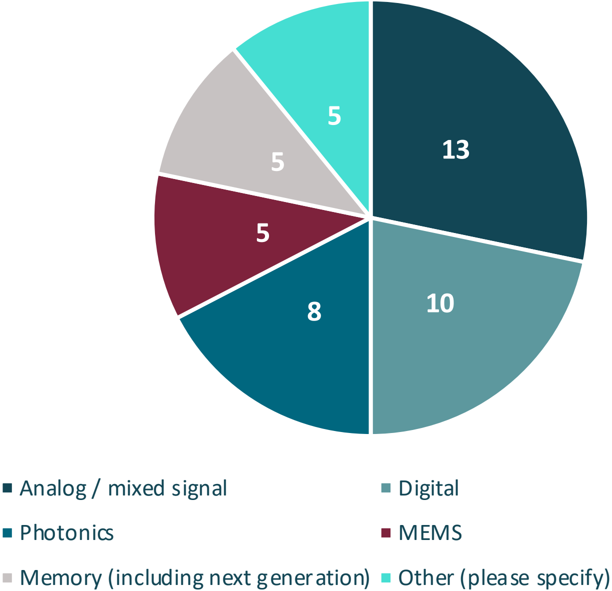
WP4 - Design IP/tooling capability

Design IP/tooling capability – User Needs

Types of chip(s) designed / developed

(Values represent number of organisations)



3-12. Priority EDA tools in terms of where you would like government support to access these capabilities.

Thermal Design
Photonics Design Tools
Packaging design
Optical Design
Open-Source Design Tools
Functional verification
Foundry PDK access
Digital Front End
Design for Manufacturing
Design Flow Methodology
Custom Layout tools
Back-end VLSI (P&R, LVS, DRC)
Analog Mixed Signal Front End

0.00 0.10 0.20 0.30 0.40 0.50 0.60 0.70 0.80

Relative importance (1=maximum)

Outsourcing and Challenges (43 respondents)

Total outsourcing activity per year	Total outsourcing activity per year **abroad**	Percentage of Design outsourced activity
£142 million	**£124 million**	25%

Top challenge	
Cost	• **High costs of EDA tools** restrict access to tools and processes and have an impact on the development and production time needed for new designs. • These leads companies to outsource these activities and potentially miss commercial opportunities. • There is an overall **impact** on companies' **productivity** and the **number of designs** that can be produced as well as the **number of designers who can be employed** by organisations

Government-sponsored Design Competence Centre

Companies supported	Design Flows offered	Support and Training	EDA Suppliers	Other Support
About **65 companies** per year Estimated to be **40%** of fabless start-ups and small SMEs	• Advanced CMOS • Standard CMOS • Optoelectronic • Power electronic • 2.5D/3D Hetero packaging	• **Design flow support** by a centralized competence design centre • **Design services** provided through the main EDA/IP vendors • EDA/IP **training** • **Tape-out** support	• Cadence • Synopsys • Siemens • Silvaco TCAD • VPI Photonics, Luceda • CST Microwave Studio	• Offer **hardware grants** to smaller companies for prototyping • Establish a **unified & simple IP framework** for NDAs, legal agreements and contracts • Coordinate the consolidation of relevant open-source IP from universities through a **national database** • Invest in **open-source tool development** and **training**

WP5 - Strategic coordination capability that would provide an institutional framework around the infrastructure components

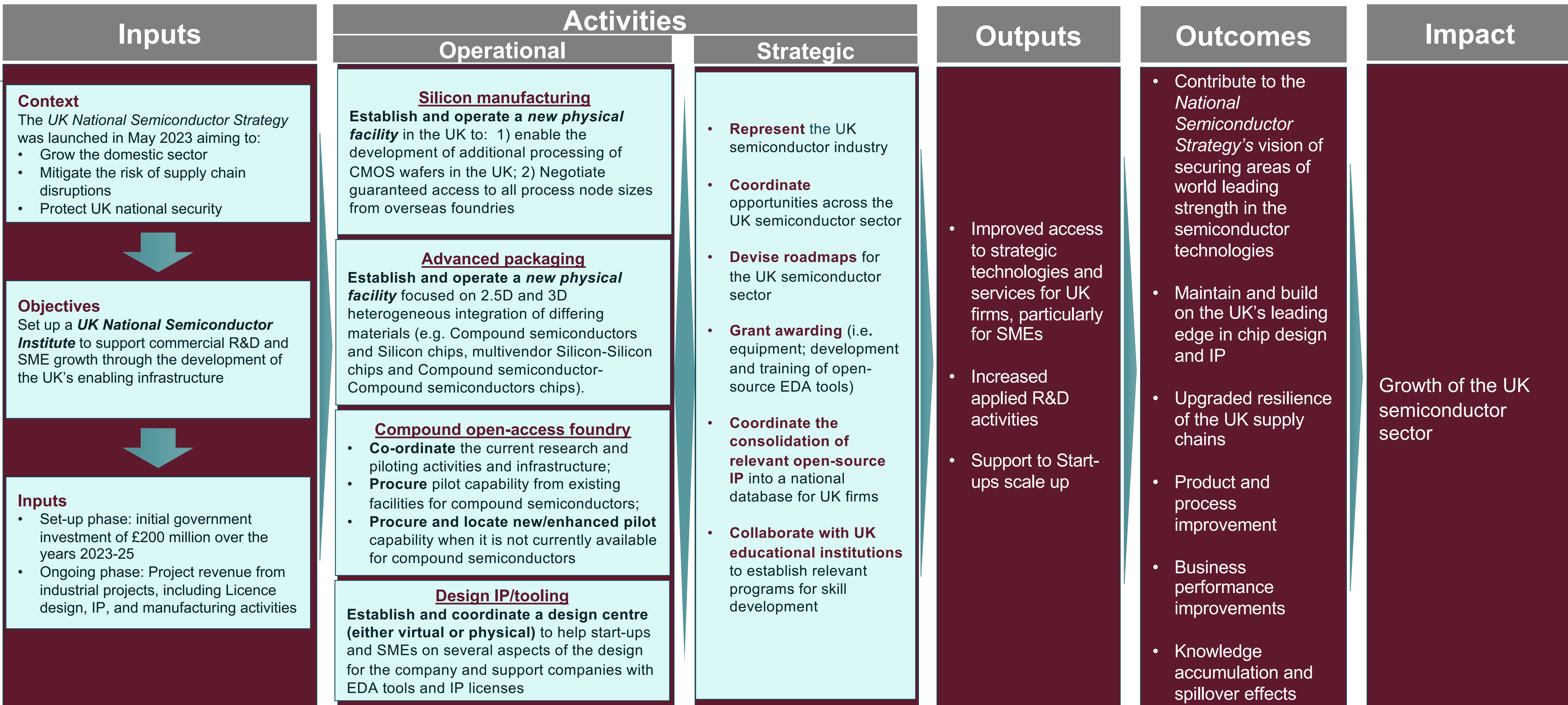
Aims

- Understand what existing **institutional frameworks** could be used to integrate the activities proposed in work packages 1 to 4 into a coherent initiative supported by the UK government by:

  1. Identifying and review relevant **organisations supporting semiconductor values chains and other sectors** in the UK, EU, Japan, Taiwan, and the US to characterise their strategic approach, business models, and innovation and coordination functions.

  2. Providing **lessons for the UK Semiconductor Infrastructure Initiative**

Semiconductor Infrastructure Initiative - the Logic Model



External factors

- Skills shortage and lack of experienced semiconductor engineers
- Misalignment between end-user requirements and manufacturing capabilities
- Access to skilled suppliers and laboratories
- IP-related constraints to access and use the required design tools and IP blocks

Review of selected organisations

- **The activities that could fall within the scope of the proposed *UK National Semiconductor Institute* are not usually conducted within a single organisation**

Two typologies of organisations have been identified:

1) **Research and Technology Organisations (RTOs)**, relying on hard infrastructure and facilities, whose primary mission is to provide key innovation services and infrastructure for enterprises.

2) **Innovation coordination organisations**, relying on light infrastructure, whose primary mission is to design long-term sectoral strategies, identify industry needs and technological priorities, provide R&D grants to other organisations, represent sector interest at national and international level, and develop support workforce development for the sector as a whole.

Review of selected organisations

The activities that could fall within the scope of the proposed UK National Semiconductor Institute are not usually conducted within a single organisation

List of UK and international organisations reviewed

Research and Technology Organisations (RTOs) Mission 1: provision of key innovation services and infrastructure for enterprises	Innovation coordination organisations Mission 2: sector long-term strategy development
• Interuniversity Microelectronics Centre – imec (Belgium) • CEA-Leti (France) • Tyndall National Institute (Ireland) • Fraunhofer Group for Microelectronics (Germany) • Leading-edge Semiconductor Technology Center – LSTC (Japan) • Industrial Technology Research Institute – ITRI (Taiwan) • Taiwan Semiconductor Research Institute – TSRI (Taiwan) • National Semiconductor Technology Center – NSTC (USA)	• Semiconductor Research Corporation – SRC (USA) • Aerospace Technology Institute - ATI (UK) • Advanced Propulsion Centre – APC (UK)

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Key findings from the international review: RTOs

- Reviewed institutions are **heavily focused on addressing the innovation needs of firms** operating both in their host country and from abroad
- Funding portfolios combine **core government funding with other income streams** such as grants and private sector contracts
- Reviewed institutions tend to be **independent and not-for-profit organisations**
- European institutions such as Tyndall, Imec, CEA-Leti and Fraunhofer are **informally part of a European distributed model** (i.e. they complement each others functions – for example firm access to facilities, EU semiconductor strategy, access to equipment)
- Reviewed institutions drive change across **three main innovation functions**: 1) knowledge generation and import; 2) knowledge mediation and diffusion; 3) knowledge supply and absorption
- The reviewed innovation centres tend to be **organised in either centralised or distributed institutional framework models**

Institutional framework options observed in international RTOs

1. **Fully centralised model,** where the following activities are concentrated in **a single location:** planning activities; decision making; business functions/departments; and physical R&D facilities and equipment
    - For example *Tyndall National Institute*

2. **Fully distributed,** empowering **geographically dispersed sub-centres** or departments to make decisions, promoting communication in all directions.
    - For example *Fraunhofer Microelectronics Group* with a contact and coordination office in Berlin and 13 financially independent centres

3. **Semi-distributed:** an organisational set-up in which **a critical mass of facilities and functions are concentrated in a single hub** that includes the organisational headquarter, while some additional facilities are distributed geographically
    - For example *imec* with a headquarter and main facilities hub located in Leuven (Belgium) plus additional distributed R&D groups and offices in foreign countries

Overall barriers where government intervention maybe required

- Skills shortage and lack of **experienced** semiconductor **engineers** available. The UK is not attractive to international talent as it offers low salaries and it has a high cost of living.
- **Standardisation of the design of electronic chip devices** which make it difficult to package them especially if chips are provided by different vendors.
- **IP issues** for accessing and using the required design tools and IP blocks. Barriers for transferring knowledge and between universities and companies. Lengthy and complicated negotiations with foundries.
- **Insufficient** allocation of **resources**/ investment especially for **scaling-up** and **manufacturing** on a large scale.
- **Misalignment** between end-user requirements and manufacturing capabilities.
- Lack of an **ecosystem** and access to facilities. There are few skilled suppliers and access to existing laboratories is difficult.

Questions

Questions