Energy beam processing and the drive for ultra precision manufacturing

An Exploration of Future Manufacturing Technologies in Response to the Increasing Demands and Complexity of Next Generation Smart Systems and Nanotechnology

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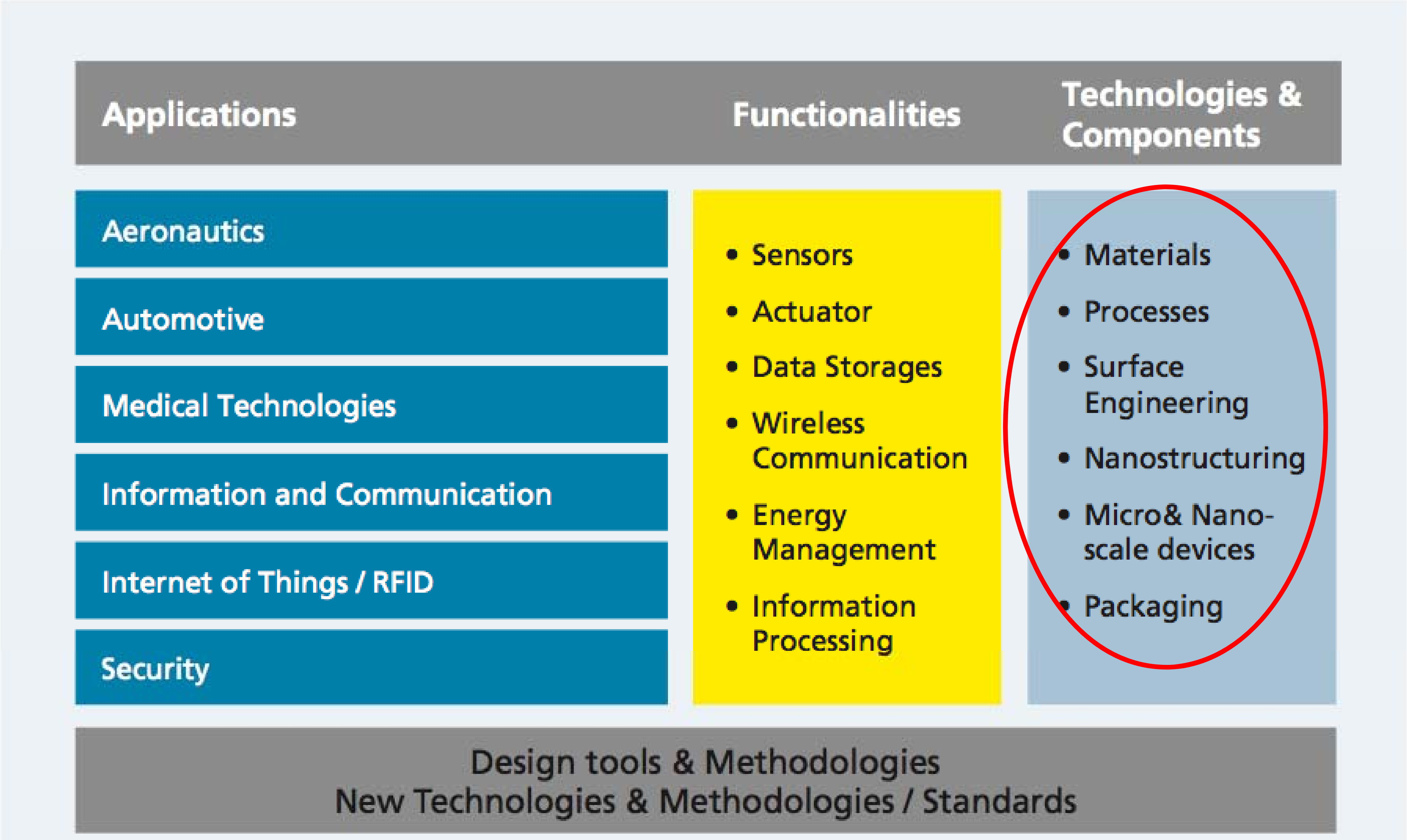
Challenges Facing Nano System Manufacturing



Applications

- Aeronautics
- Automotive
- Medical Technologies
- Information and Communication
- Internet of Things / RFID
- Security

Functionalities

- Sensors
- Actuator
- Data Storages
- Wireless Communication
- Energy Management
- Information Processing

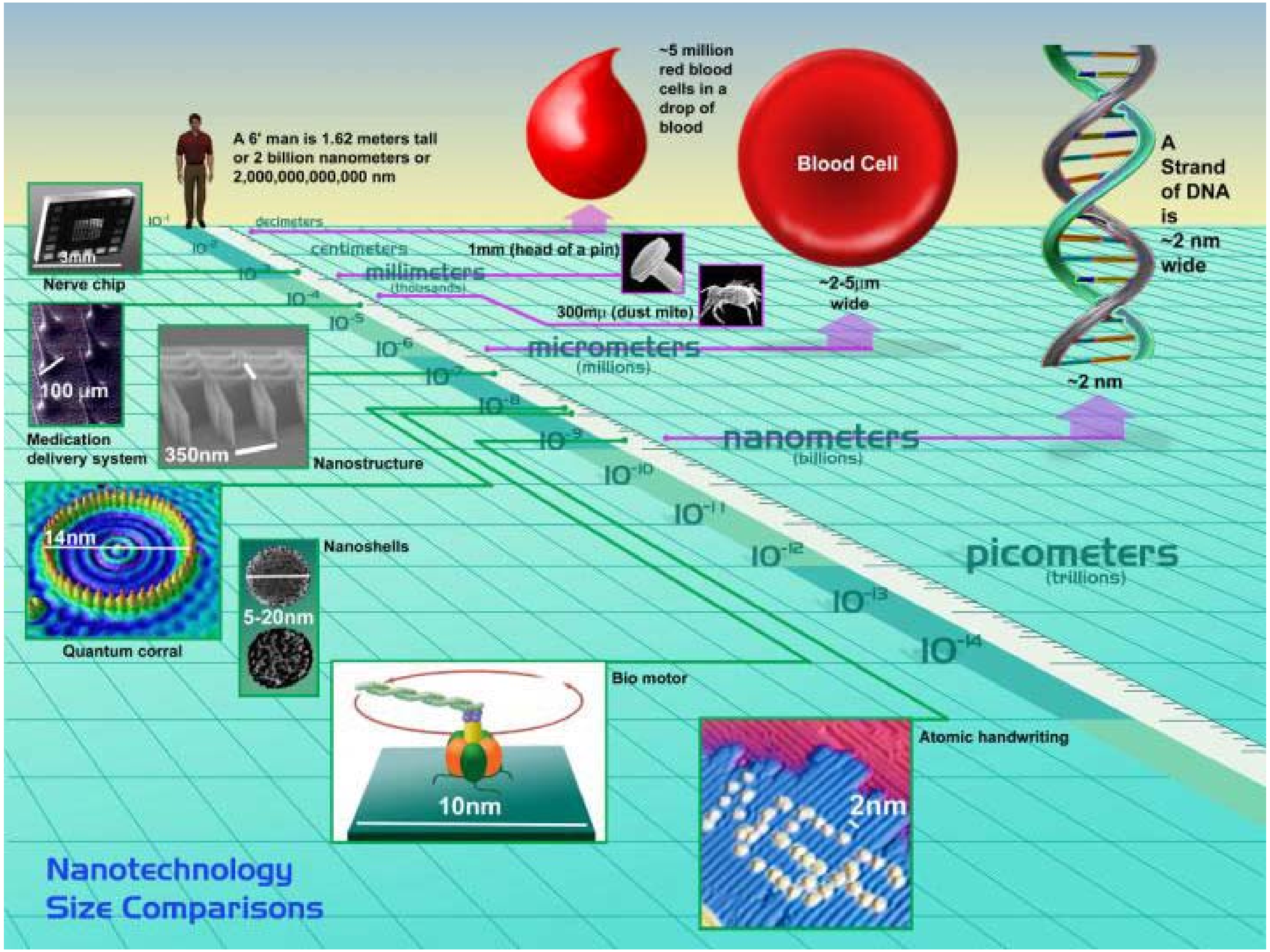
Technologies & Components

- Materials
- Processes
- Surface Engineering
- Nanostructuring
- Micro& Nano-scale devices
- Packaging

Design tools & Methodologies
New Technologies & Methodologies / Standards

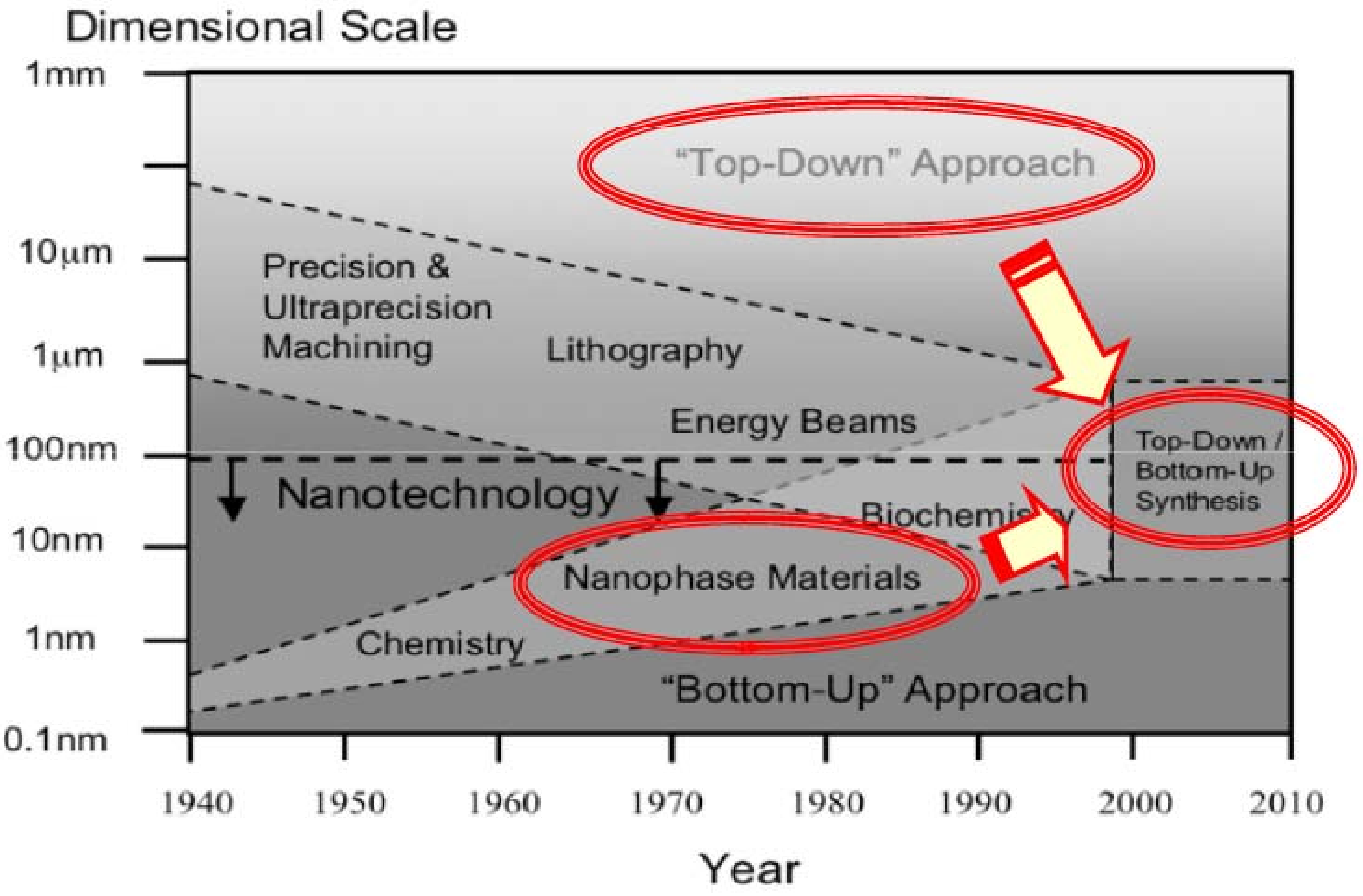
Strategic Research Agenda, EPoSS, v2 2009

Manufacturing length scales..



http://nanopedia.case.edu/NWPage.php?page=nanoscale

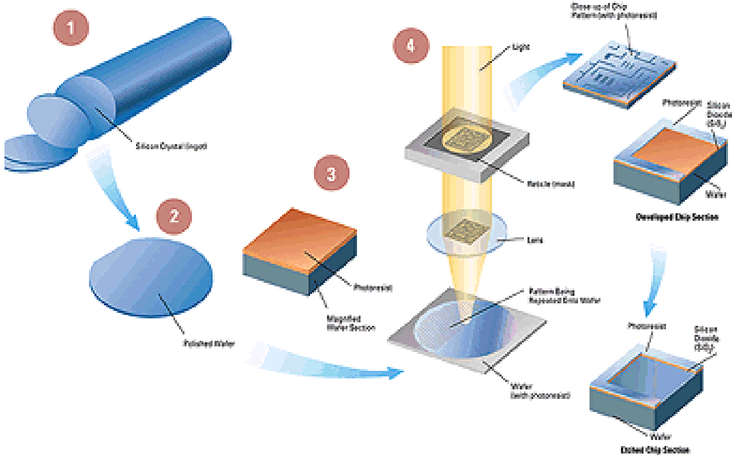
Manufacturing Methodology vs Length Scales



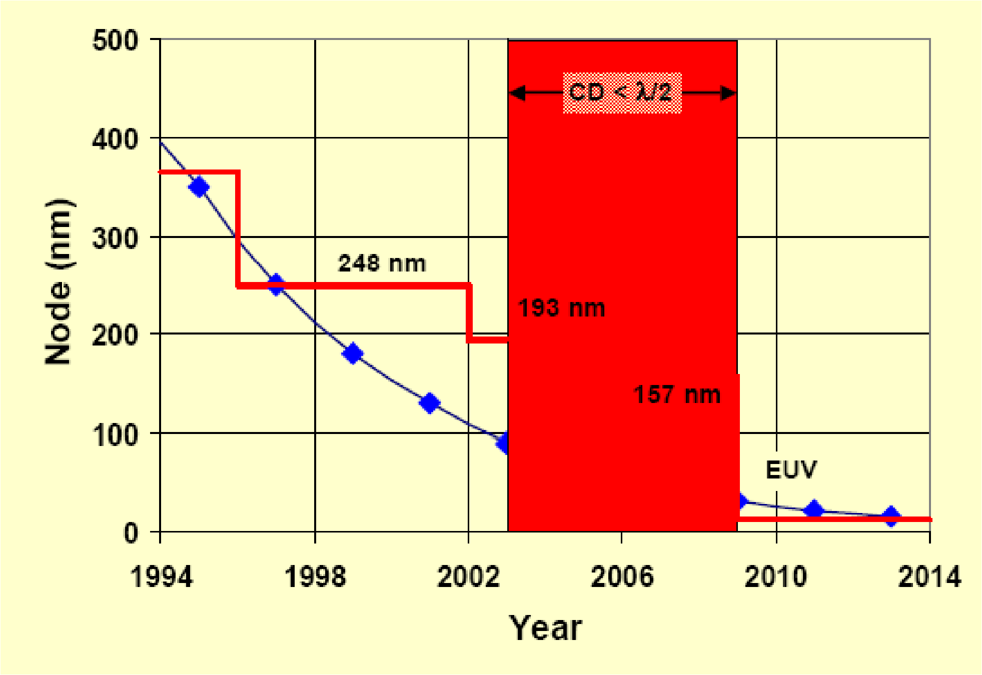
Nanoscience and nanotechnologies,
The Royal Society & The Royal Academy of Engineering (www.nanotec.org.uk)

Lithographic techniques

- Lithography is the principle means of writing circuit elements
- Resolution limited by wavelength

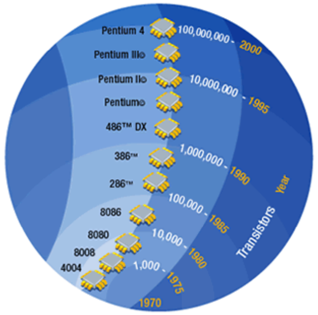


Optical Lithography
Feature Size vs Wavelength



INTERNATIONAL SEMATECH

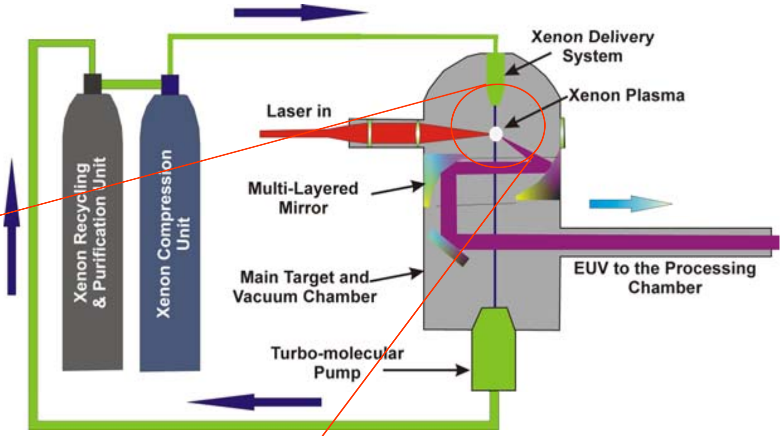
X-ray lithography

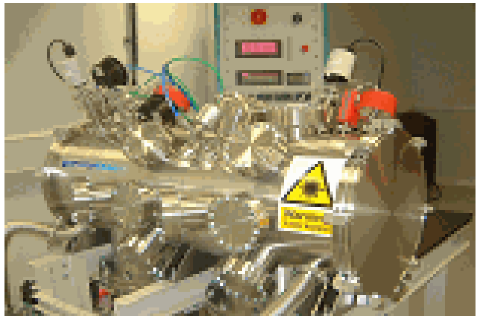


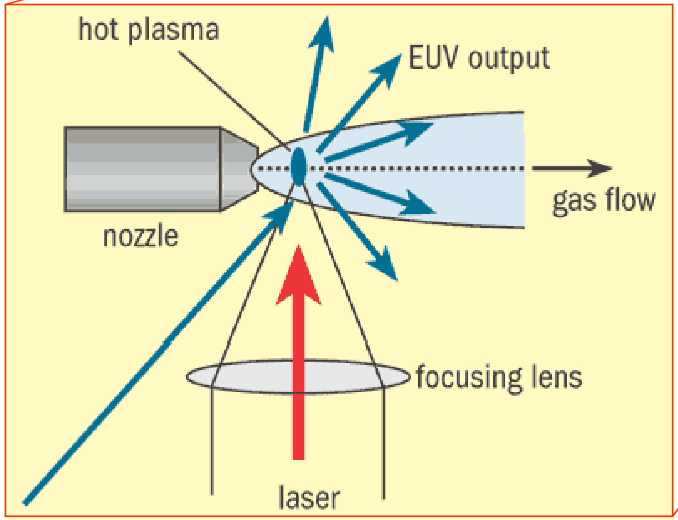
Moores Lawe

EUV Source Production

In conformance with Intel co-founder Gordon Moore's 1965 prediction, now known as "Moore's Law," the density of circuit elements on microchips has doubled roughly every 12 to 18 months for more than 30 years, resulting in ever smaller, faster, and cheaper computers. However, manufacturers know that the traditional technique for printing circuit patterns—optical lithography based on refractive optics (lenses)—cannot continue indefinitely on this course







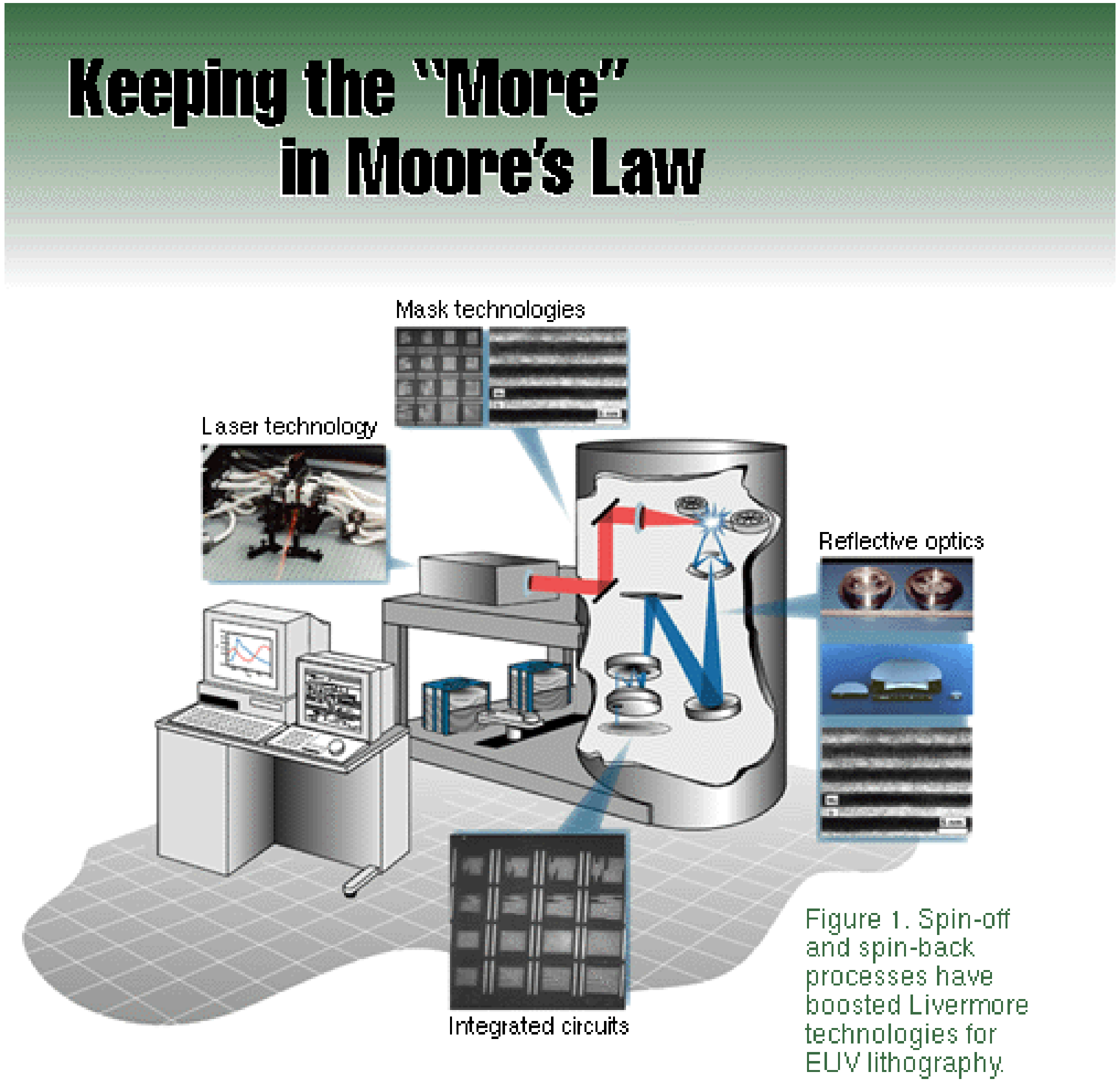
Today's leading candidate for a successor, known as EUV lithography, relies on reflective optics (mirrors) to image patterns from masks onto the surface of a silicon wafer that will ultimately be diced into microchips. The first computer processors produced with EUV technology beginning around 2007 are expected to be almost ten times faster than today's most powerful chips, and the storage capacity of memory chips will increase even more. But before that day arrives, there is the matter of producing accurate EUV lithography cameras

EUV Source Requirements

- **100W at the workpiece (λ 13.5nm)**
- **Pulse repetition > 1kHz**
- **Chamber pressure < 10^{-6} bar**
- **Xenon density 10^{18} cm^{-3}**
- **Laser power density 10^{11} to 10^{13} Wcm^{-2}**

powerlase

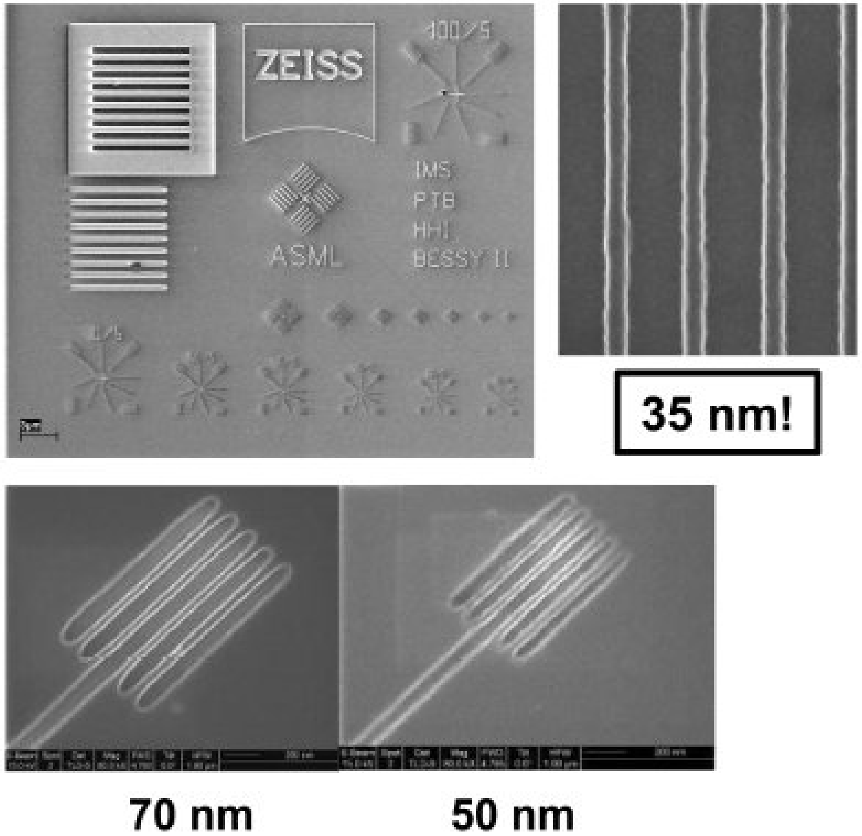
BOC EDWARDS



Keeping the "More" in Moore's Law

Figure 1. Spin-off and spin-back processes have boosted Livermore technologies for EUV lithography.

http://www.llnl.gov/str/Sweeney.html

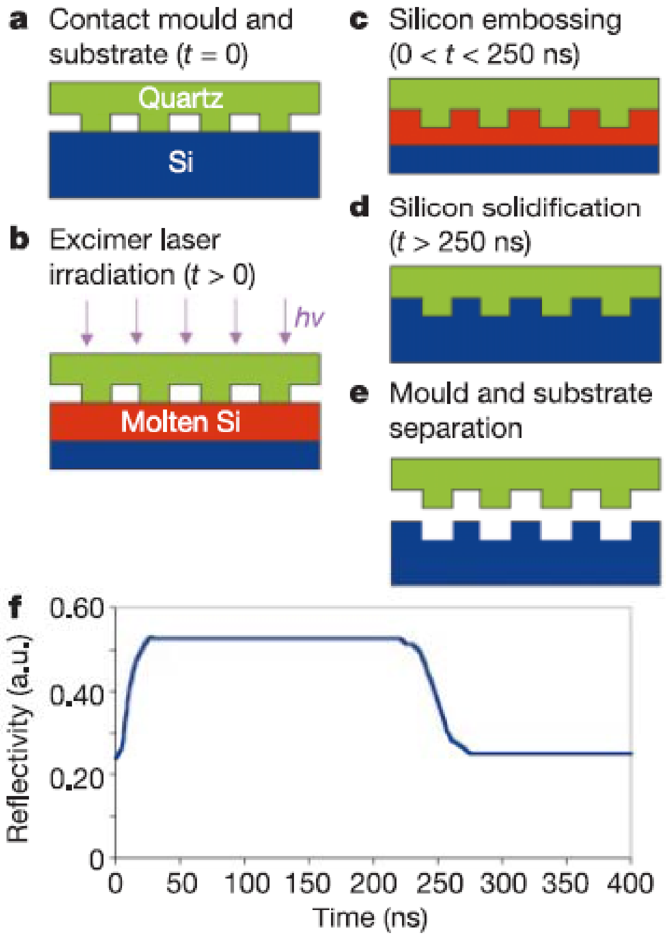


Carl Zeiss SMT AG has demonstrated that the EUVL technology is capable of fulfilling the requirements to print semi-dense lines down to 35nm and below

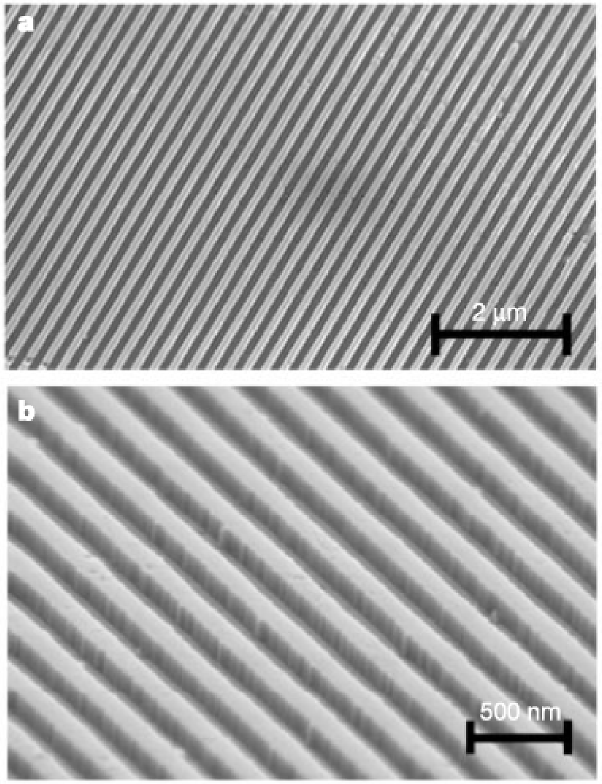
ASML

EUV on track
for commercial use

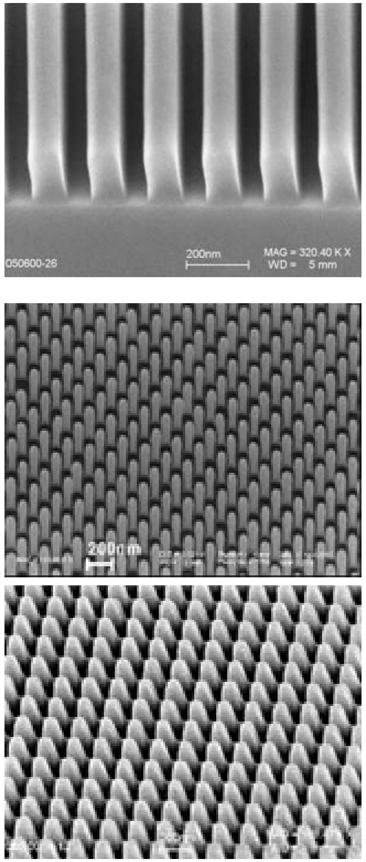
Long term future? Nano Imprint Lithography



Stephen Y. Chou*, Chris Keimel & Jian Gu
NanoStructure Laboratory, Department of Electrical Engineering,
Princeton University, Princeton, New Jersey

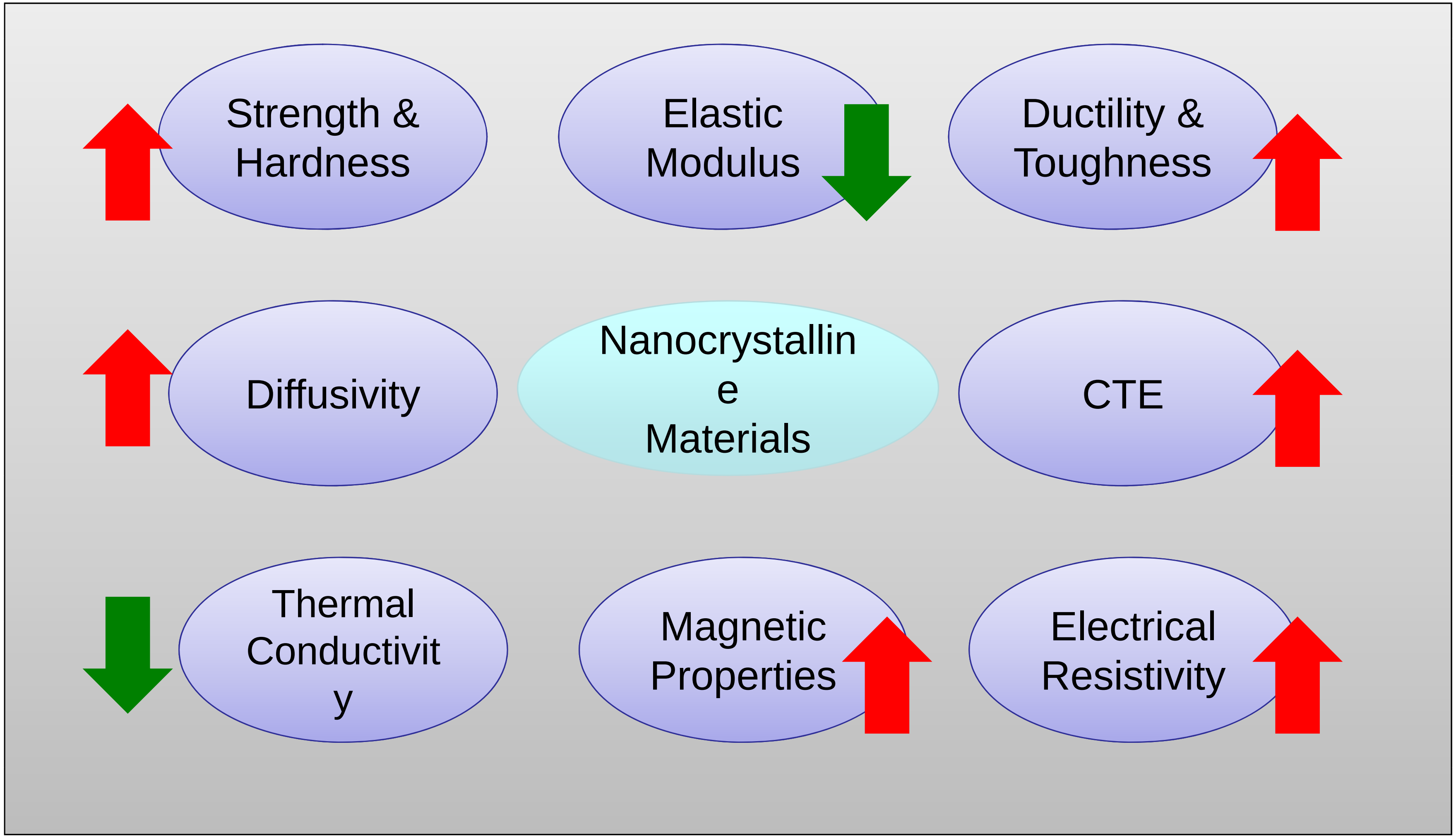


Scanning electron microscope (SEM) images. a, A uniform 300 nm period silicon grating patterned by LADI. The grating has 140 nm linewidth and is 110 nm deep. b, The mould after the two LADI processes showing no visible damage.



>10 nm !!

Nanophase material properties in comparison with coarse grained counterparts



↑ Strength & Hardness

Elastic Modulus ↓

Ductility & Toughness ↑

↑ Diffusivity

Nanocrystalline Materials

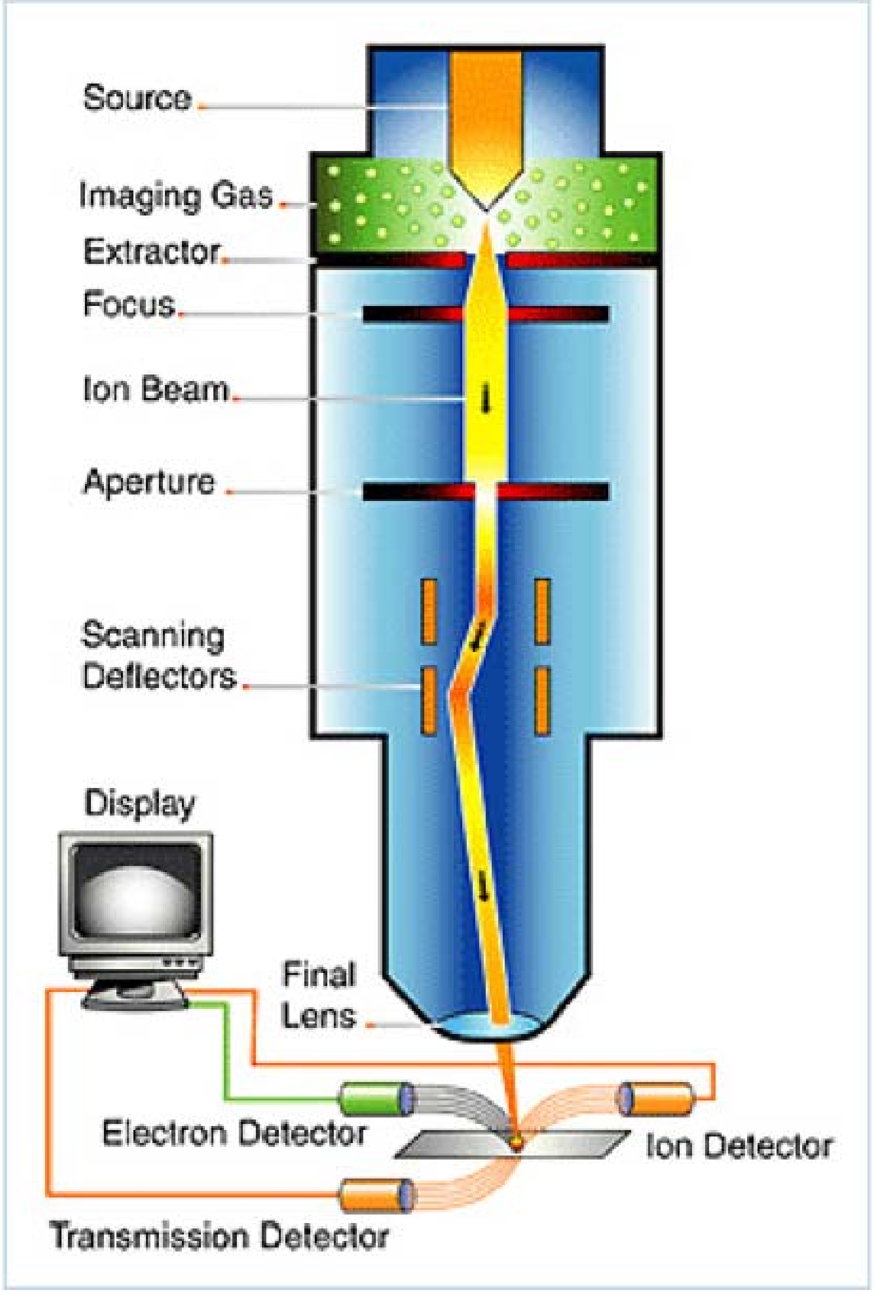
CTE ↑

↓ Thermal Conductivity

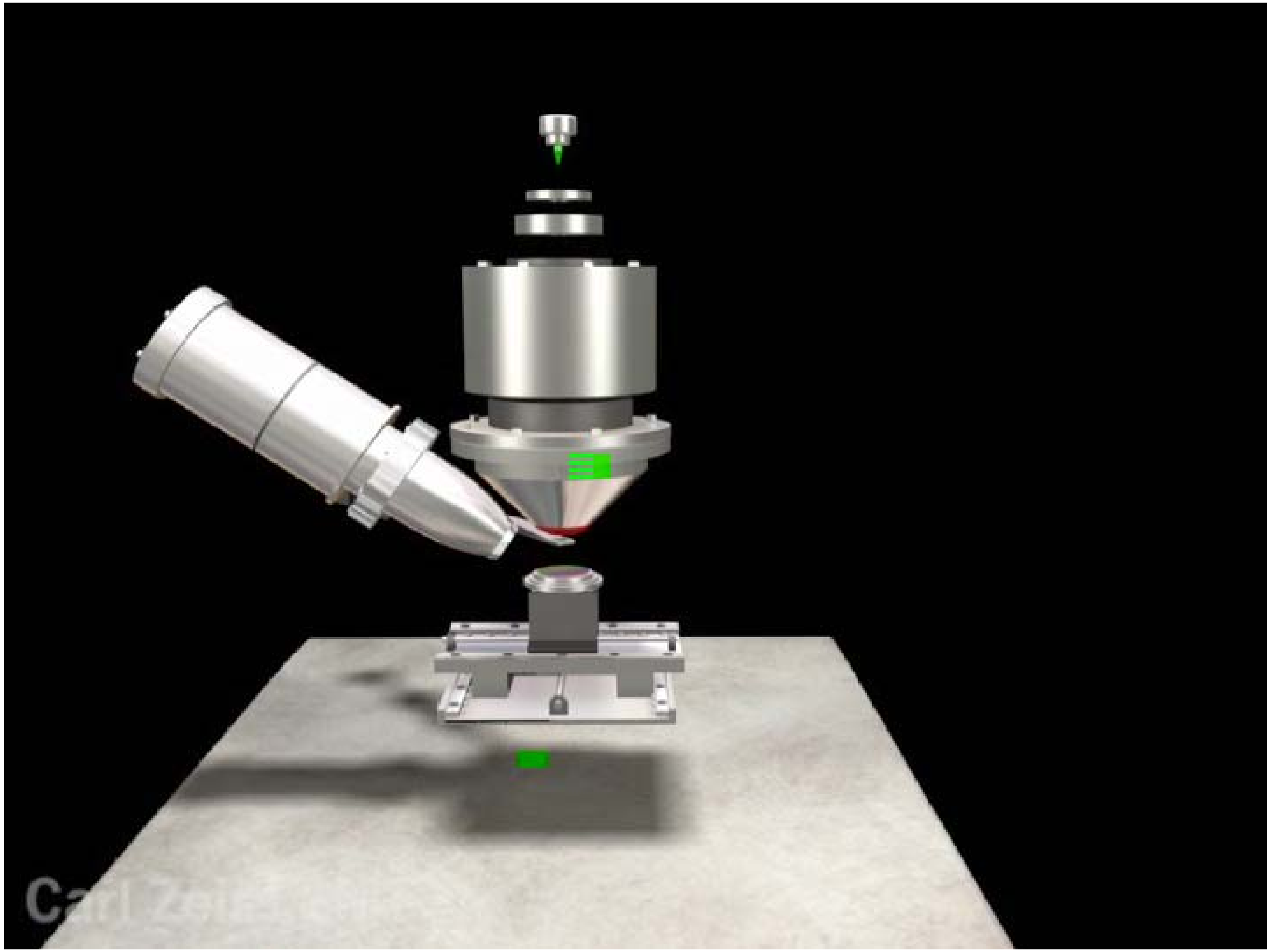
Magnetic Properties ↑

Electrical Resistivity ↑

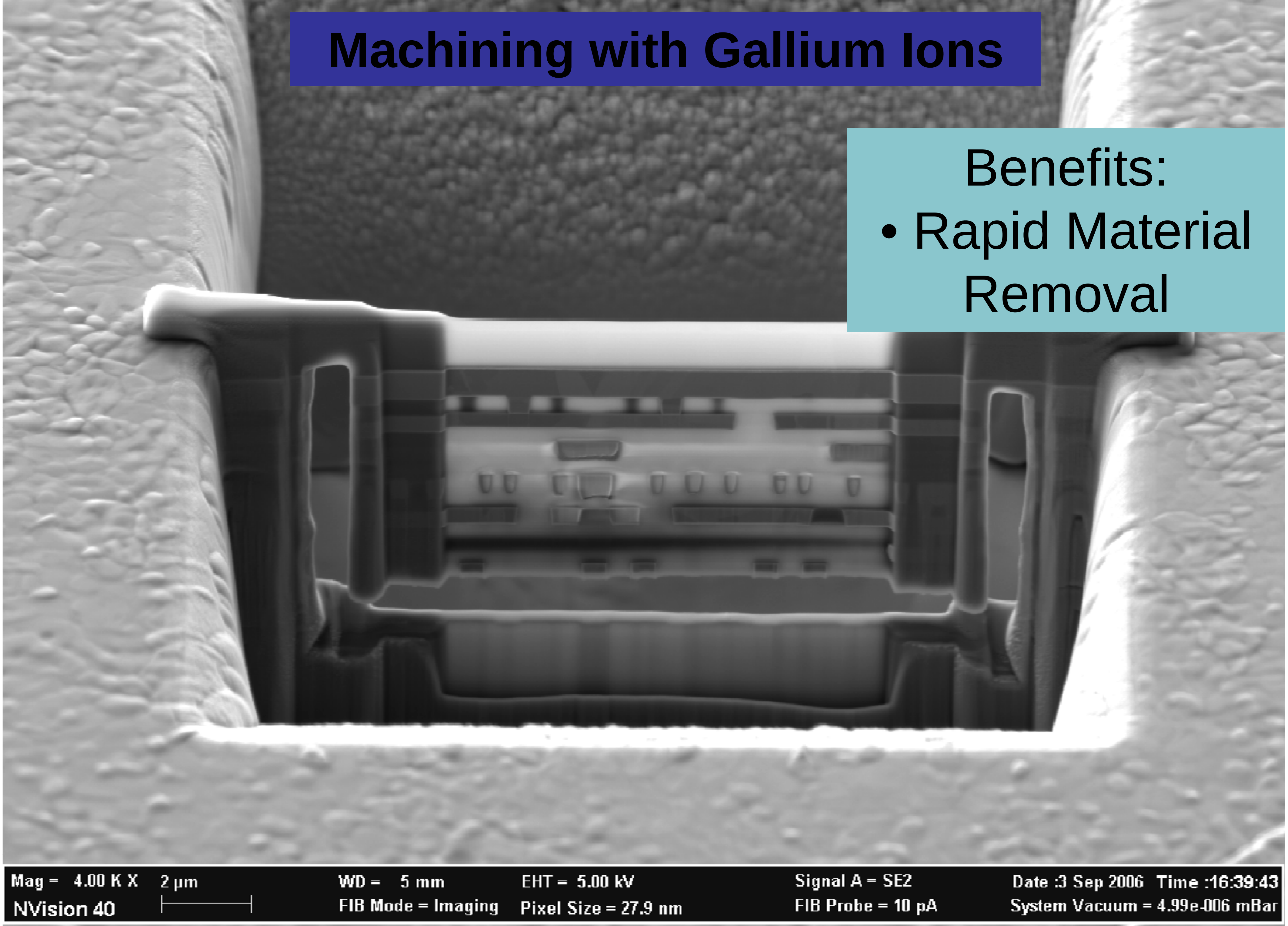
Focused Ion Beam



Ga Focused Ion Beam Machining



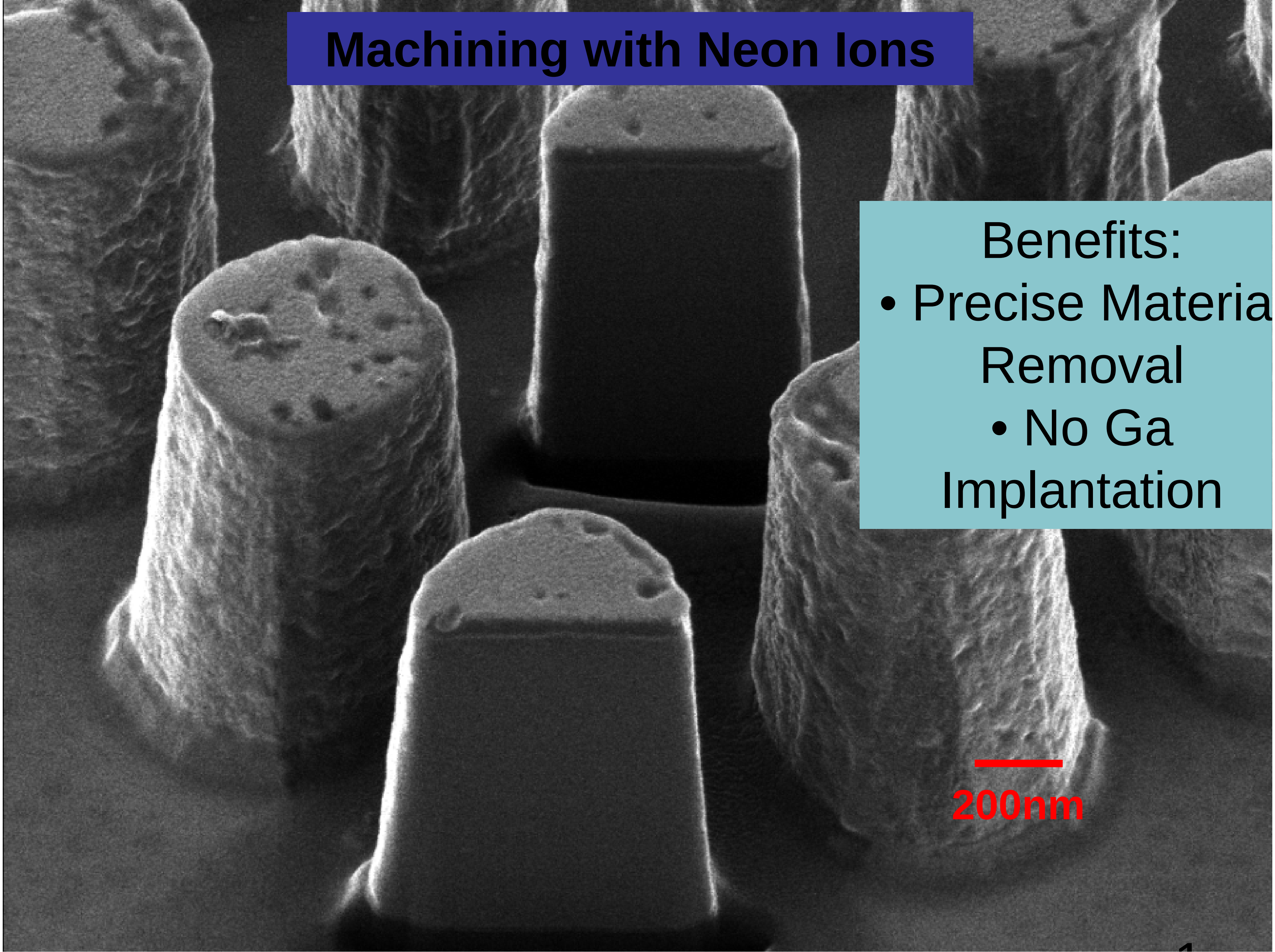
Machining with Gallium Ions



Benefits:

- Rapid Material Removal

Machining with Neon Ions

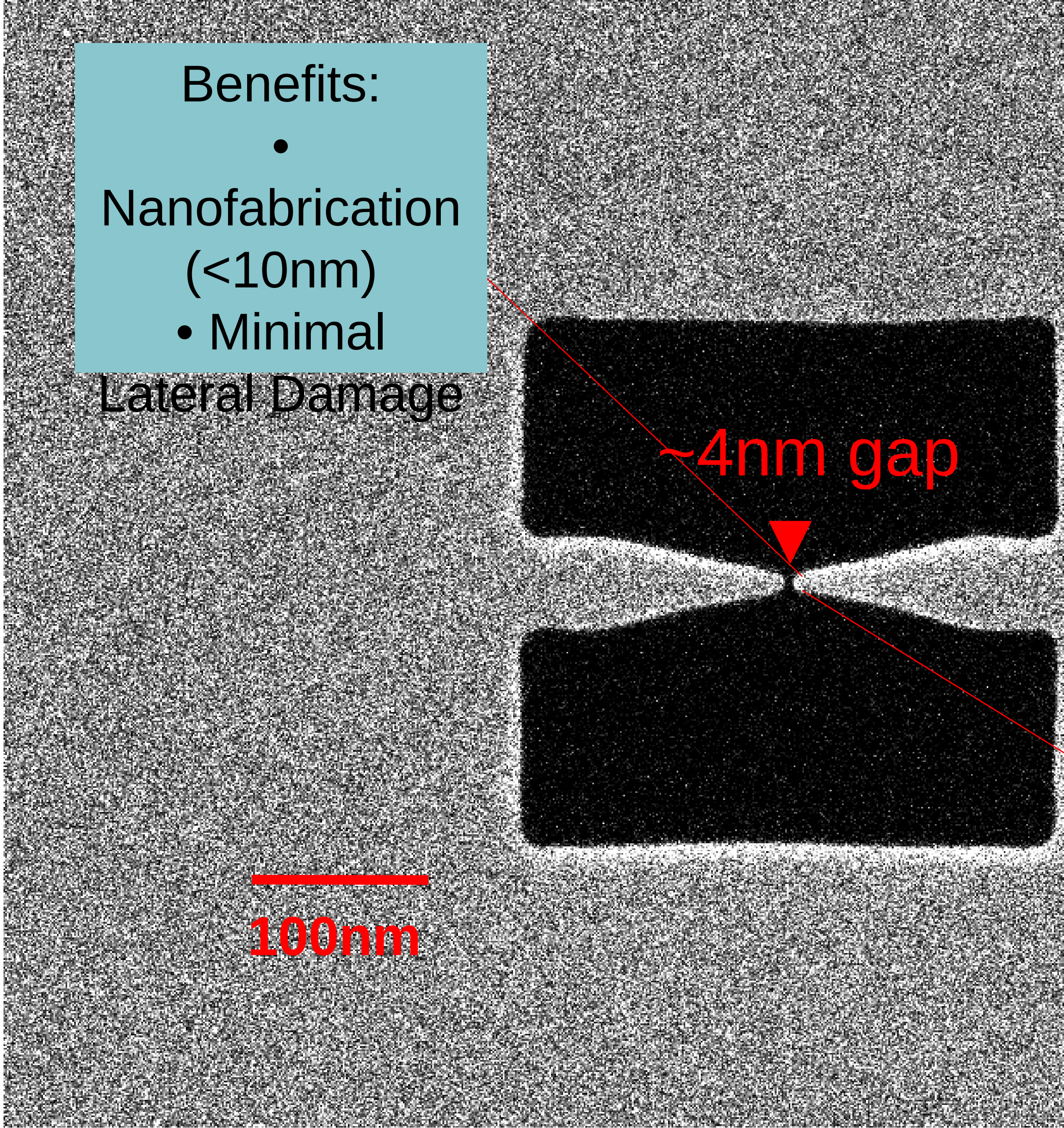


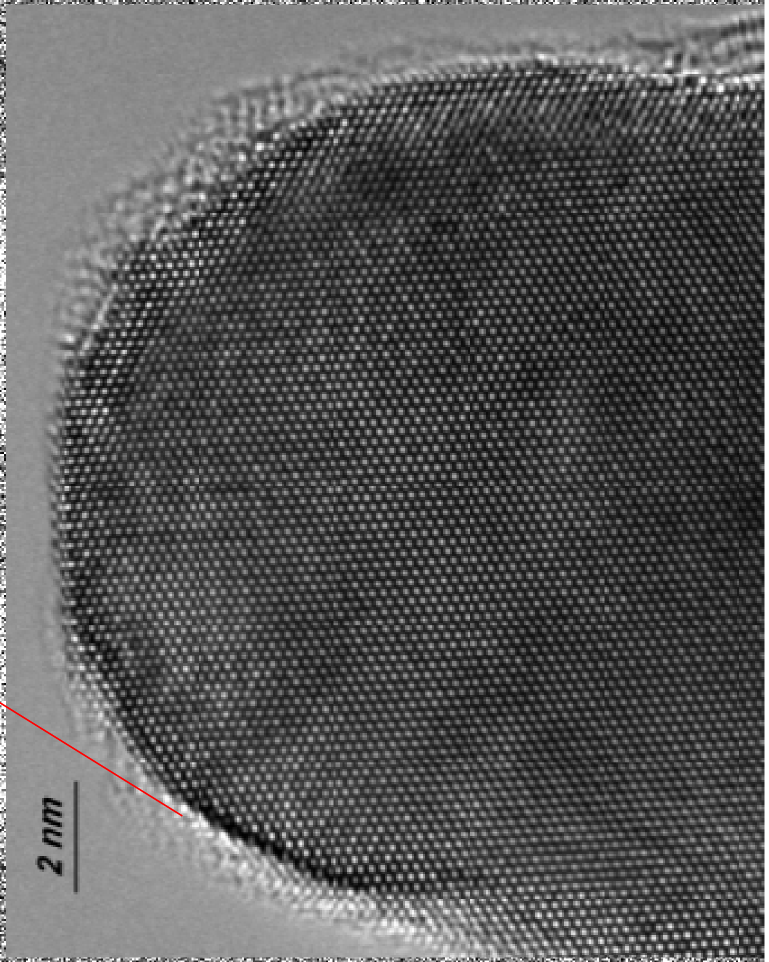
Benefits:

- Precise Materia Removal
- No Ga Implantation

Machining with Helium Ions

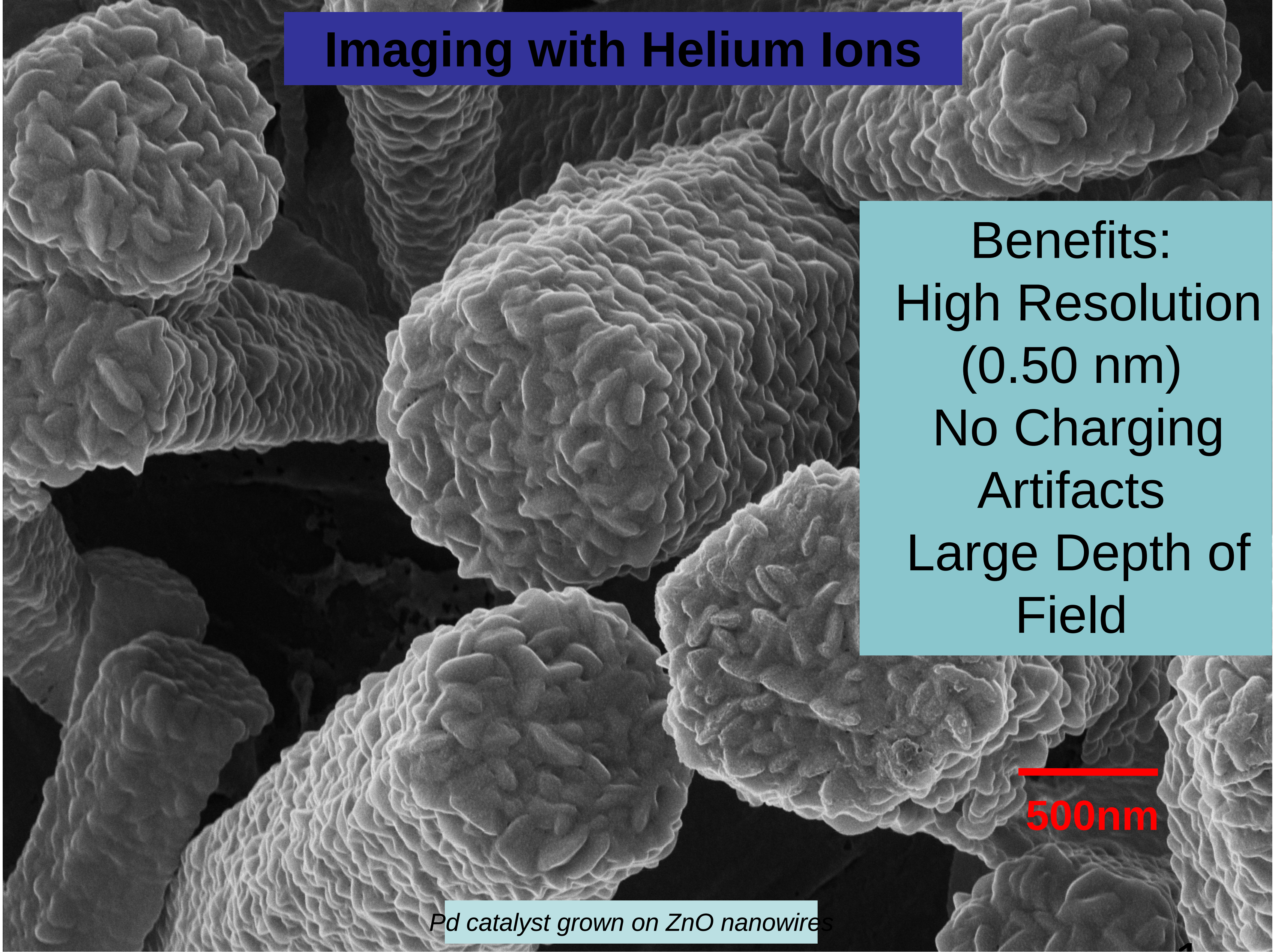
Benefits:
- Nanofabrication (<10nm)
- Minimal Lateral Damage


~4nm gap



TEM Image

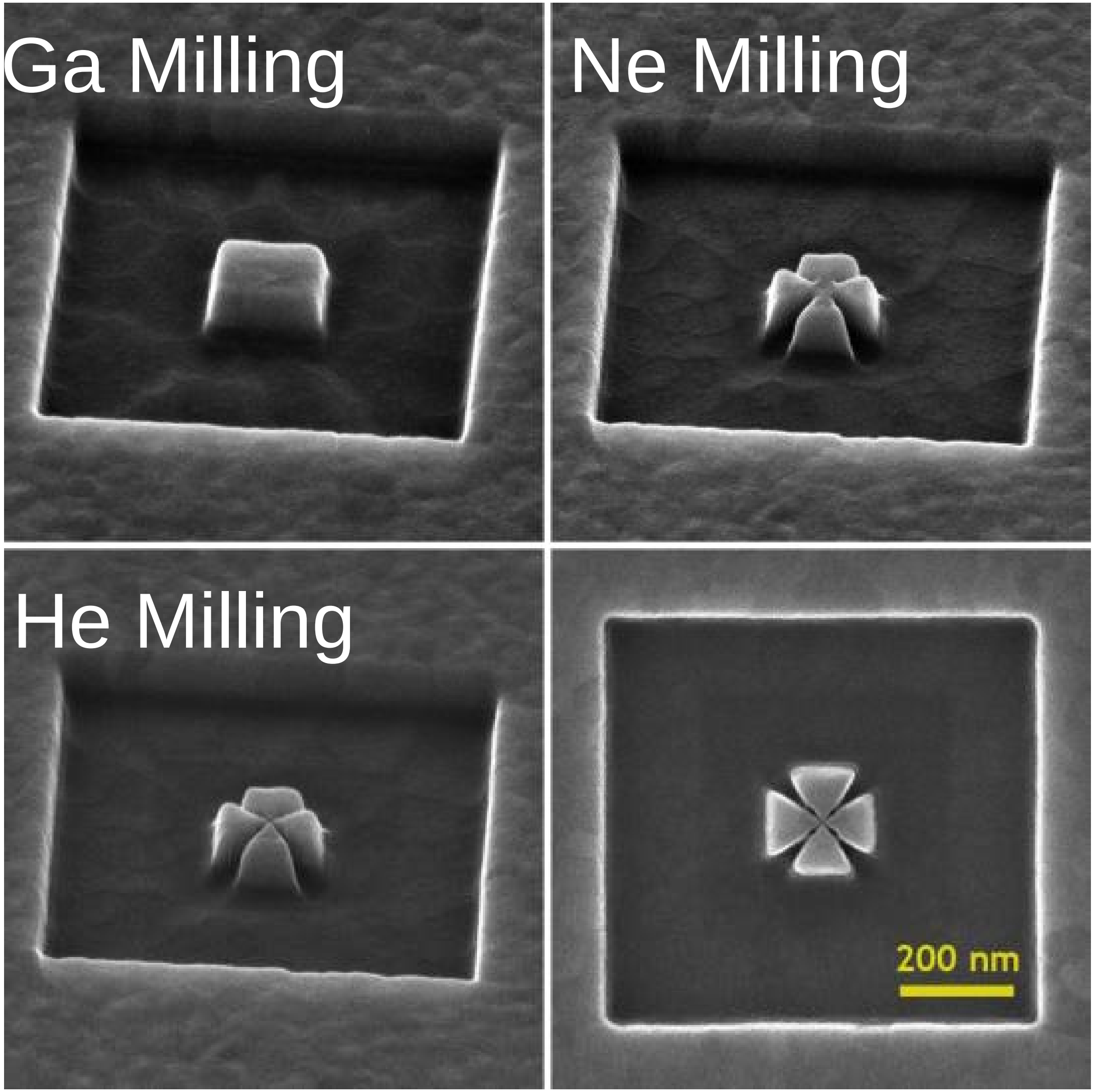
Imaging with Helium Ions



Benefits:
High Resolution (0.50 nm)
No Charging Artifacts
Large Depth of Field

Pd catalyst grown on ZnO nanowires

Multi-ion beam machining



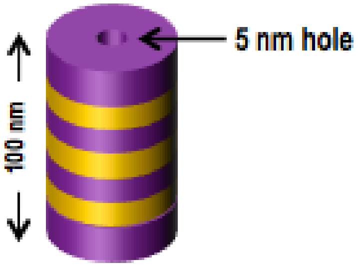
Sample: Gold film on Glass substrate

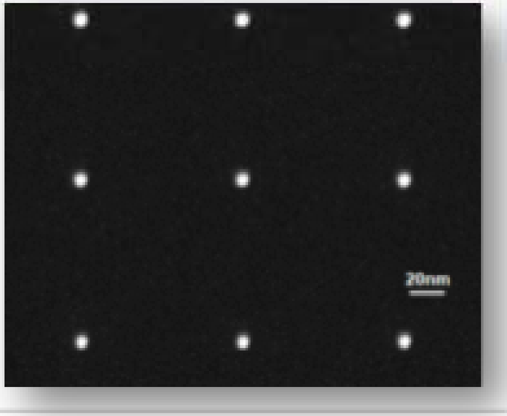
Ion Beam Milling
Application • *Solid State Nanopores*

Research Area	DNA sequencing, Single Molecule Detection
Challenge	Creating 5 nm holes in 7 layer metal-dielectric sandwich film
Conventional Method	TEM at high energy

Solution	**Helium Ion Beam Milling, 400X faster**

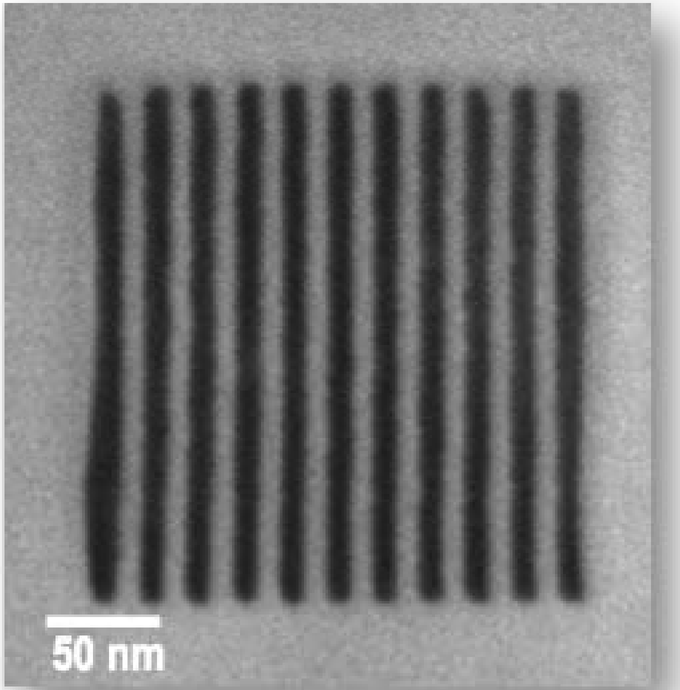
- **15s to drill a single hole (400X faster than TEM).**
- **Hole uniformity much better than any other technique (± 1nm variability).**





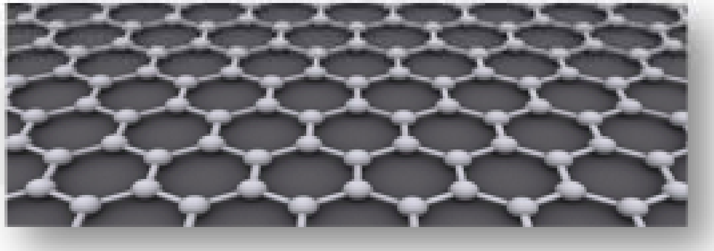
Ion Beam Milling
Application • *Graphene Nanoribbons (GNR)*

Solution **Helium Ion Beam Milling**



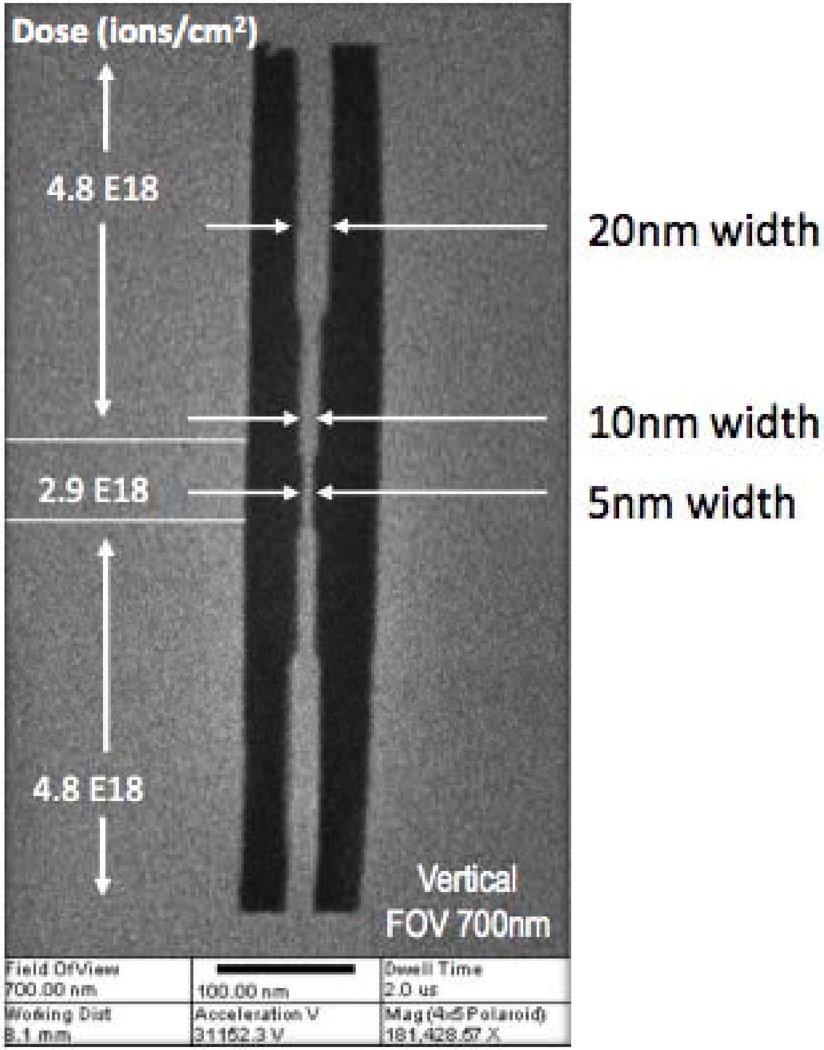
**Courtesy: Dan Pickard, NUS*

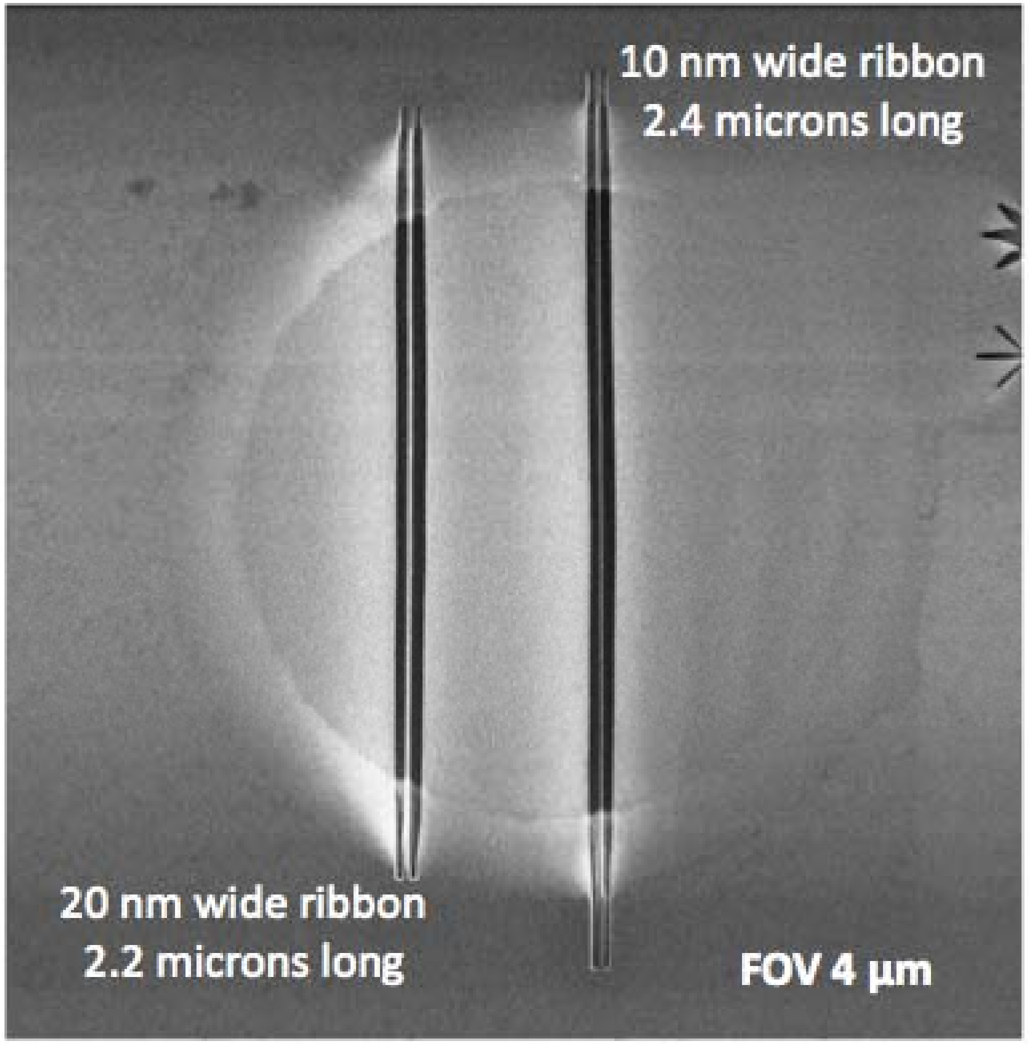
- Graphene created by the exfoliation method
  - 1-3 layers thick
- Created on SiO_2 over cylindrical holes on surface.
- Ion milling carried out on the suspended area.



Advantages Fast, non-destructive, contamination-free

He Ion Beam Milling
Graphene Nanoribbons (GNR)

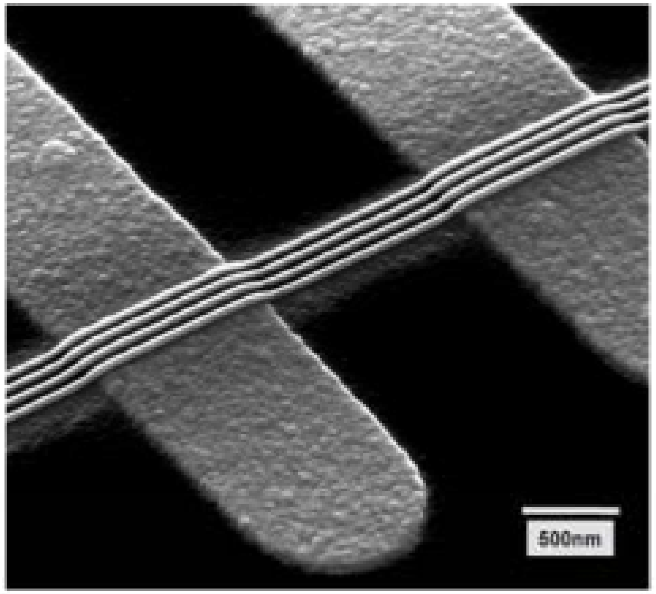




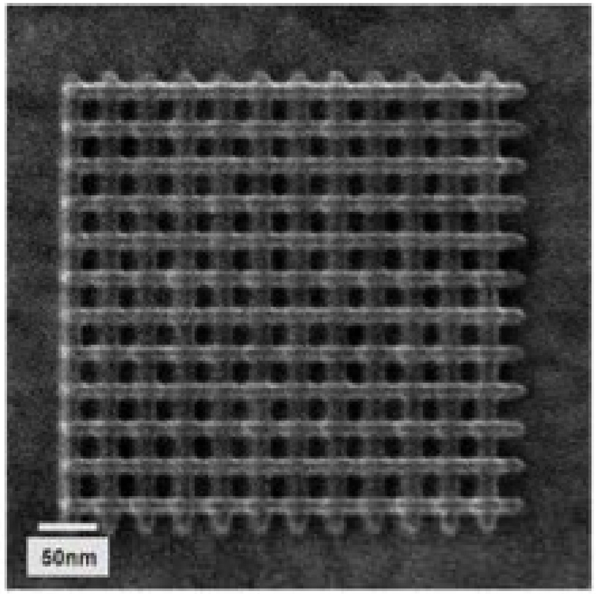
Courtesy: Dan Pickard, NUS

Ion Beam Induced Deposition
Application • Deposition and Etching of Metals/Insulators

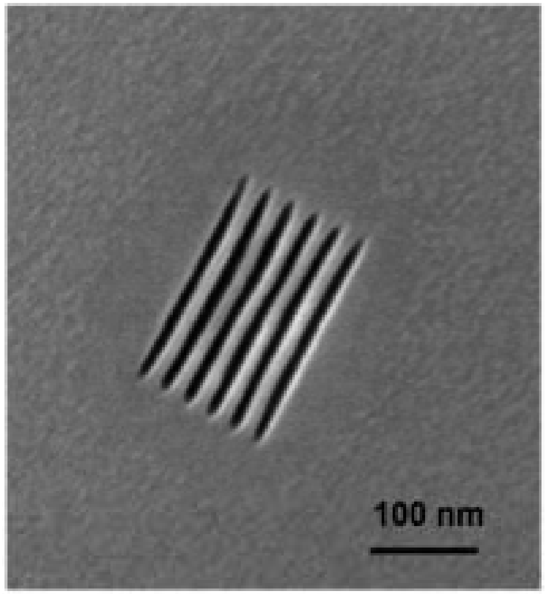
Research Area	Semiconductor failure analysis
Challenge	Creating high quality metal and insulator deposits for the 22nm node and beyond
Solution	**He/Ne Ion Beam Induced Deposition**



50nm metal lines with 100uΩ.cm resistivity



15nm insulators with $10^{11}\Omega$.cm resistivity

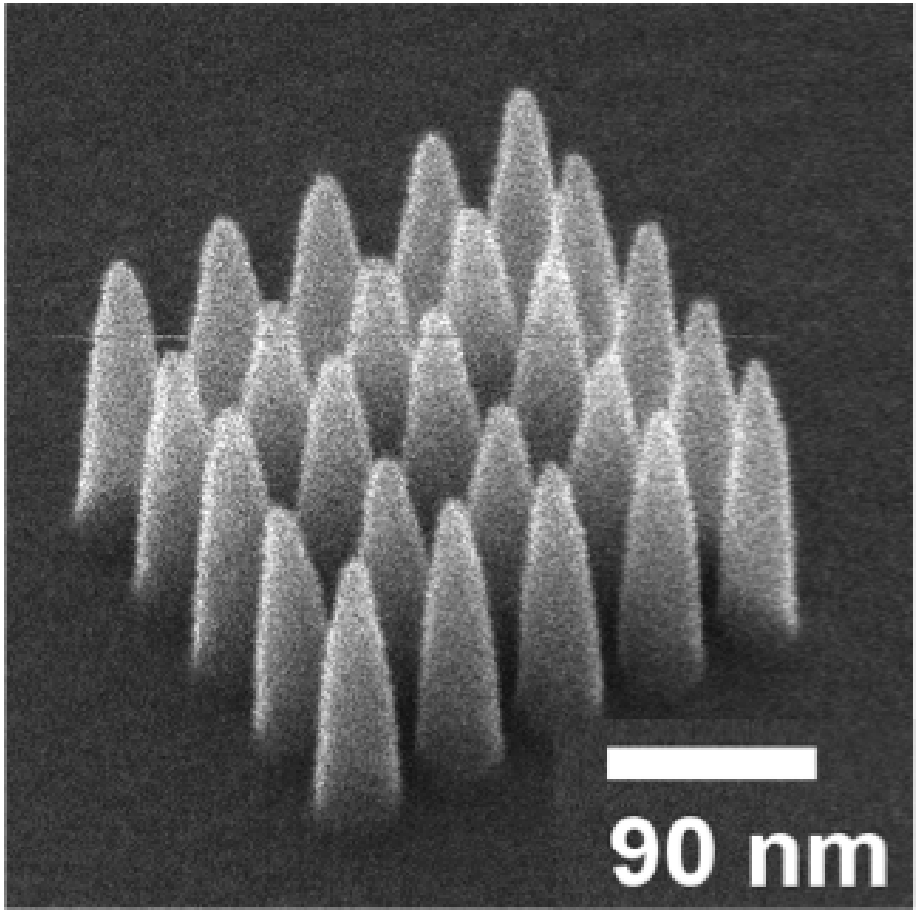


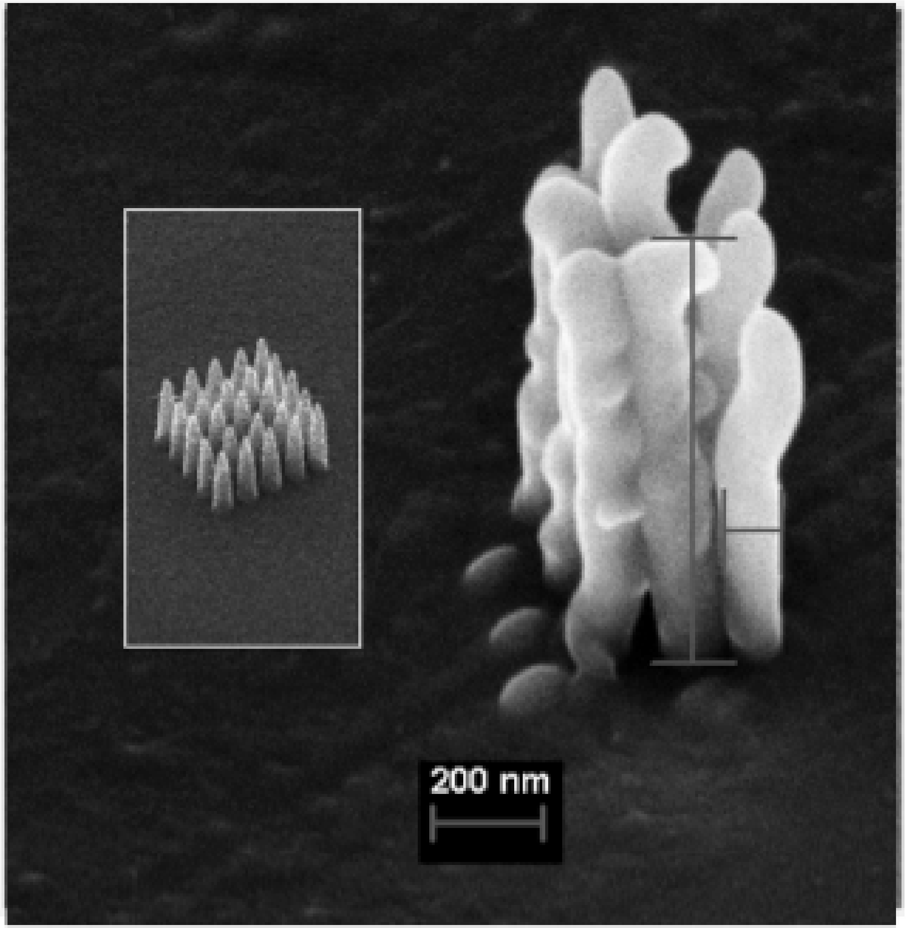
12nm lines etched in TaN absorber layer

Ion Beam Induced Deposition

Pillar Growth: Proximity Effects

- FIB: minimum pillar diameter > 100 nm
- HIM grown: 35-40 nm
- 200nm pitch Ga-deposited pillars are severely distorted by neighbor interactions
- Helium pillars grow uniformly at 16x packing density

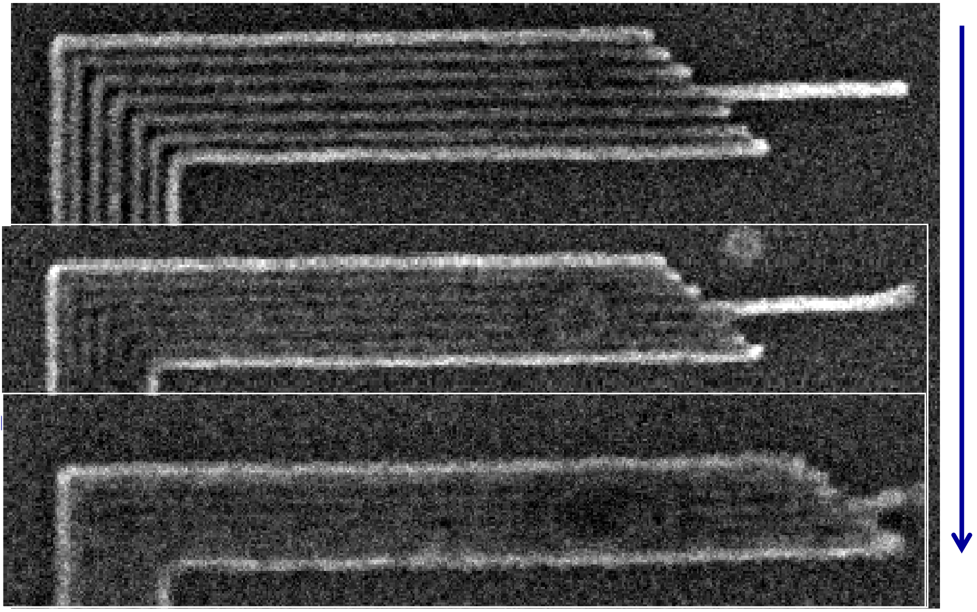




Ion Beam Lithography

Application • *Sub-10 nm Lithography*

Solution	Helium Ion Beam Lithography.
State-of-the-art He-Beam Litho	Best results : 4 nm lines at 7 nm pitch



Half-pitch = 5 nm
Dose = 68 ions/nm

Half-pitch = 4 nm
Dose = 56 ions/nm

Half-pitch = 3.5 nm
Dose = 49 ions/nm

Extending the limits…

Source: Karl Berggren, MIT
Donny Winston, HP

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EPSRC
Pioneering research
and skills

UNIVERSITY OF
CAMBRIDGE

EPSRC Centre for Innovative Manufacturing in Ultra Precision

SAMSUNG

JAGUAR

Microsharp

fives cinetic

HEXAGON METROLOGY

NPL

M-SOLV Limited

NOKIA
Connecting People

SPI

PQL

ZEISS

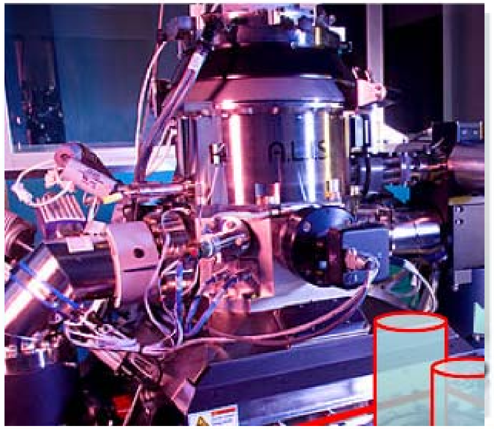
Key Research Challenges

Create & demonstrate new production chains to apply **nano & micro scale** features rapidly onto large (and continuous) **multi-material substrates**, through “ flag ship ” projects creating 3 research platforms.

Create & demonstrate new ultra precision and fine feature generation processes for **multi-material processing** of emerging smart products including their **effective quality control**.

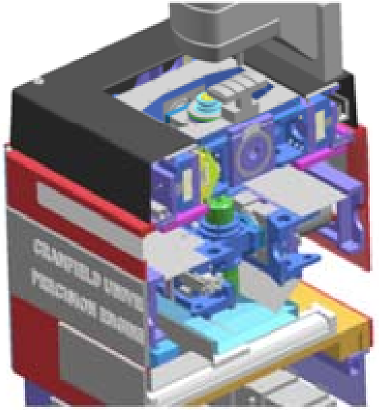
Ultra Precision Technologies

Next generation ion-beam
Nano fabrication systems



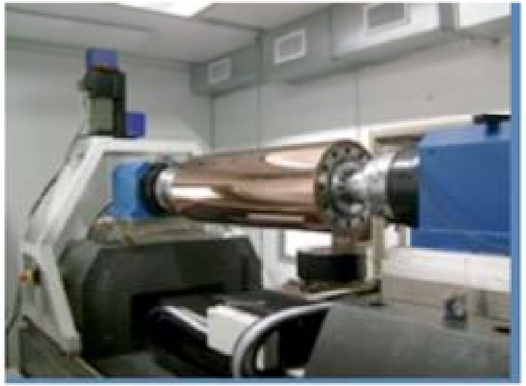
Working envelope
100x100x100mm

Next generation laser
Micromachining systems



Working envelope
100x100x100mm

Large scale nano/micro
Reel-reel production



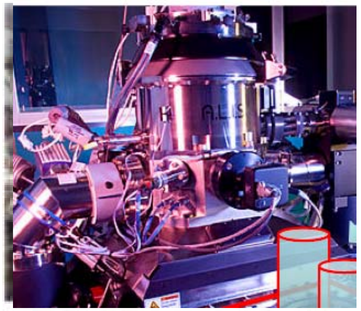
Working envelope
1.5x1x1m

Nanometer precision

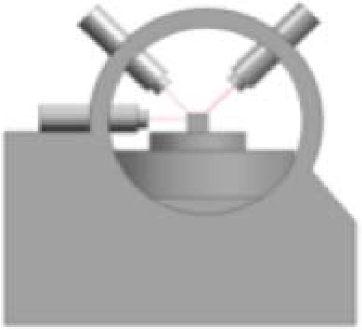
Closed loop manufacturing processes

Quantum electronics, nano-photonics, displays, holographic optics, micro-fluidics, polymer electronics, precision optics, micro-components, optoelectronics

Research Platforms

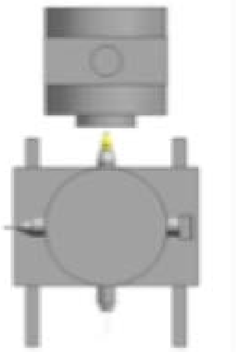


Plasma, Laser, Ion



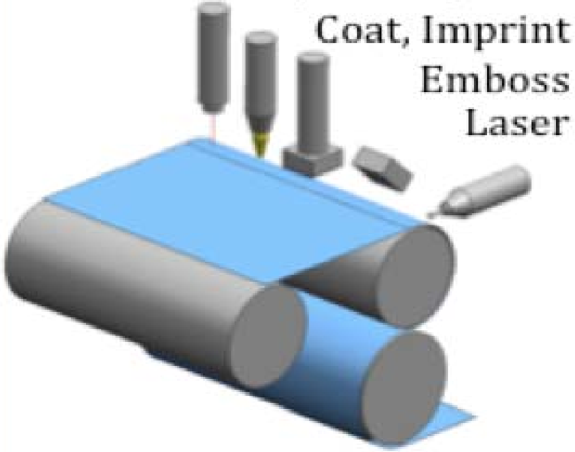
Nano FIB
Platform
(vacuum)

Diamond, Plasma,
Print, Imprint
Coat, Laser



Meso scale
Platform
(atmospheric)

Diamond, Plasma, Print
Coat, Imprint
Emboss
Laser

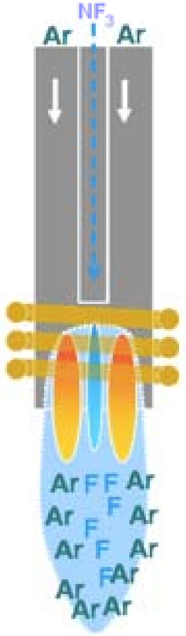


Macro “r2r”
Platform
(atmospheric)

Nano Fabrication Platform Technology

ZEISS

Ultrafast Laser surface/
volume modification



RAP surface/volume
sputtering

High resolution system
integration

Productivity ~ x 30,000 over FIB

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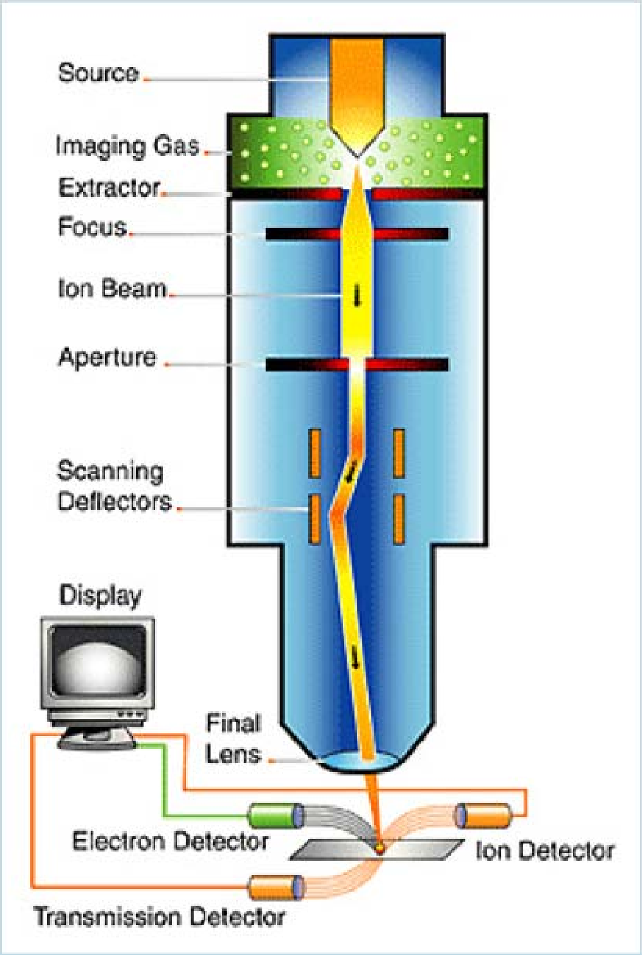
Hybrid FIB/Laser/RAP

Laser & Reactive Atom Plasma Processing stations



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The Alpha Factory

- The Alpha Factory would serve as a hub for innovation and manufacturing technology development and company scale up and would actively identify and provide services required to support client's success. Preliminary objectives for the Centre may include the following:
- Assist the commercialisation of emerging innovation
- Support the development of advanced manufacturing technologies
- Create new job opportunities for Cambridge area residents and those in the wider UK
- Better leverage of intellectual property from universities, research laboratories and companies
- Generate new innovation models for the UK

Bibliography

1. CMOS Process Flow in Wafer Fab, Semiconductor Manufacturing Technology, DRAFT, Austin Community College, January 2, 1997.

2. Semiconductor Processing with MKS Instruments, Inc.

3. Worthington, Eric. “New CMP architecture addresses key process issues,” *Solid State Technology*, January 1996.

4. Leskonic, Sharon. “Overview of CMP Processing,” SEMATECH Presentation, 1996.

5. Gwozdz, Peter. “Semiconductor Processing Technology” SEMI, 1997.

6. CVD Tungsten, Novellus Sales Brochure, 7/96.

7. Fullman Company website. “Fullman Company - The Semiconductor Manufacturing Process,” http://www.fullman.com/semiconductors/index.html, 1997.

8. Barrett, Craig R. “From Sand to Silicon: Manufacturing an Integrated Circuit,” *Scientific American Special Issue: The Solid State Century*, January 22, 1998.

Thank-you